

Embedding and Verification of PSL using ASM

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Abstract— In this paper, we propose a methodology to integrate the Property Specification Language (PSL) in the verification process of systems designed using Abstract States Machines (ASMs). We provide a specification of PSL in ASM, which allows us to integrate PSL properties as part of the design. For the verification, we propose a technique based on the AsmL tool that translates the ASM code (containing both the design and the properties) into a finite state machine (FSM) representation. We use the generated FSM to run model checking on an external tool, here SMV. Our approach takes advantage from the ASM language capabilities to model designs at the system level as well as from the power of the AsmL tool in generating both a C# code and an FSM representation from an ASM model. We applied our approach on SystemC designs, which are translated into ASM models. Experimental results on a bus structure from the SystemC library showed a superiority of our approach to conventional verification.

I. INTRODUCTION AND MOTIVATION

Abstract State Machines (ASM) [7] is a formal specification method for software and hardware systems that has become successful for specifying and verifying complex systems. The ASM formalism is used as a modeling language in a variety of domains both in academic and industry contexts [9]. The ASM methodology is mathematically precise, yet general enough to be applicable to a wide variety of problem areas. The ASM thesis asserts that any computing system can be described at its natural level of abstraction by an appropriate ASM. ASMs provide features to capture the behavioral semantics of programming and modeling languages, as a wide range of these languages were defined with this notion [9]. There are many languages that have been developed for ASMs, the recent one is AsmL [11] which was developed at Microsoft Research. We chose this language, as a common level of abstraction, to define an abstract simulator, and then model designs and properties. AsmL [3] is integrated with Microsoft's software development environment, where it can be compiled and connected to the .NET framework. AsmL effectively supports specification and rapid prototyping of different kinds of models. The AsmL tester can also be used to generate finite state machines (FSMs) or test cases.

The Accellera Property Specification Language (PSL) [13] was developed to address the lack of information about properties and design characteristics of RTL (register transfer level)

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models. It provides means of specifying design properties using a concise syntax with clearly defined formal semantics. PSL permits the specification of a large class of design properties at four layers: Boolean, temporal, verification and modeling layers. It is intended to be used for functional specification to capture requirements regarding the overall behavior of a design in one hand, and as an input to verification tools using simulation or formal verification on the other hand.

In this work, we propose an embedding of PSL in ASM with an approach to verify properties on design implementations. We embed PSL properties in ASM to be able to reason about the behavior of the design and its correctness against its specification. We use the AsmL tool [11] in order to generate an FSM of the design model (including the properties). This approach enabled the verification of PSL properties on designs using classical model checking tools, for example SMV [10]. For this, we translate the generated FSM into the input language of the SMV tool.

Figure 1 shows a sketch of our methodology for the embedding and verification of PSL in ASM, where the contributions of this paper are indicated by a dashed box. We applied our approach to designs modeled in SystemC [14], which are translated into ASM [2][8]. We used the bus structure of the SystemC library to show the feasibility and performance of our approach. The experimental results proved the practicality of our methodology as a solution to the verification problem of SystemC designs.

The rest of the paper is organized as follows: Section 2 presents related work to ours. Section 3 describes our embedding for PSL in ASM. In Section 4 we provide an application for our approach to SystemC verification with a case study to illustrate our methodology. Finally, Section 5 concludes the paper and points to a few future work directions.

II. RELATED WORK

In [6], Gordon used the semi-formal semantics in the PSL/Sugar documentation [13] to create a deep embedding of the whole language in the HOL theorem prover [5]. The author developed the formal definition of the full PSL language in HOL. The combination of PSL/Sugar and higher-order logic is quite expressive and provides temporal logic constructs as higher level syntactic sugar for higher order-logic, thereby enabling properties to be formulated elegantly. Gordon *et al.* [4] described how to 'execute' the formal semantics of PSL

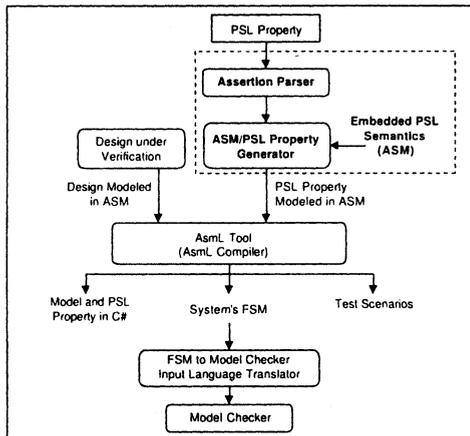


Fig. 1. Methodology for verification of PSL in ASM.

using HOL and investigated the feasibility of implementing useful tools to conduct automatic verification of PSL from the formal semantics. They implemented two experimental tools: an interpreter that evaluates whether a finite trace, satisfies a PSL formula, and a compiler that converts PSL formulas to checkers in an intermediate format suitable for translation to HDL to be included in simulation test-benches. However, they did not provide any framework for the verification of PSL for any implementation language.

In a similar work, Claessen and Martensson [1] defined an operational semantics for a weak fragment of PSL, the safety property subset, and then proved the correctness of these semantics with respect to a denotational semantics. They do not provide definitions for all PSL operators like clock operators and sequential composition, and yet, there is no execution for these semantics that provides verification solution.

Wallace [15] used the ASM notation to define operational semantics of C++ programming language focusing on its object oriented and other advanced features like classes, inheritance, operator overloading, virtual functions, templates, and exception handling. Definitions for other languages semantics such as Prolog, SDL, and Standard ML using ASM can be found in [9]. These semantics definitions provide no execution of the language semantics itself in order to give a solution to design problems like verification.

III. EMBEDDING PSL IN ASM

PSL is an implementation independent language to define properties (also called assertions). It does not replace, but complements existing verification methodologies like VHDL and Verilog test benches. PSL presents a different view of the design and may imply FSMs in the implementation. The syntax of PSL is very declarative and structural which leads to sustainable verification environments. Both VHDL and Verilog flavors are provided. PSL consists of following four layers: **The Boolean layer** builds expressions that are used in other layers, specifically the temporal layer. Boolean expressions are

evaluated in a single evaluation cycle.

The temporal layer is used to describe properties of the design in addition to simple properties. This layer can describe properties that involve complex temporal relations. Temporal expressions are evaluated over a series of evaluation cycles.

The verification layer is used to tell the verification tool what to do with the properties described by the temporal layer.

The modeling layer is used to model behavior of design inputs for formal verification tools, and to model auxiliary parts of the design that are needed for verification.

This layered approach allows the expressing of complex properties from simple primitives. A property is built from three types of building blocks: Boolean expressions, sequences, which are themselves built from Boolean expressions, and finally subordinate properties. Sequences, referred to as SEREs (Sequential Extended Regular Expressions), are used to describe a single- or multi-cycle behavior built from Boolean expressions.

There are two ways to embed PSL properties into the design, either into the design code itself or by adding them as external monitors. We adopted the first approach, where all the parameters of PSL properties are defined as objects. The objective of the embedding is to reuse PSL properties, as embedded in ASM, at lower design levels since the AsmL tool can automatically compile them into a C# or .NET code. This latter code can be compiled and executed with the concrete SystemC level.

A. Boolean Layer

This layer is the basic layer of PSL. Even though it is called *Boolean layer*, it includes types other than Boolean such as integers and bit vectors. We embedded this layer in ASM by defining classes for all types and expressions including their methods. Our embedding is based on the semi-formal semantics presented in the reference manual [13], and the formal semantics definition in HOL [6].

The embedding of the PSL Boolean layer mainly includes:

- 1) *Expression type class* includes the basic 5 types: *Boolean*, *PSLBit*, *PSLBitVector*, *Numeric* and *String*. Both *Boolean* and *String* types are directly inherited from the ASM's *AsmL.Boolean* and *AsmL.String*, respectively. The *PSLBit* type is constructed using the enumerated structure *One*, *Zero*, *X*, and *Z*. The *PSLBitVect* type extends the *PSLBit* type and offers additional operations such as access to the bit vector contents. Finally, the *PSLNumeric* type extends the *AsmL.Integer* type (*AsmL.Integer*) by adding some conversion methods from *PSLBitVector* to integers and vice-versa.
- 2) *PSL Expressions* construct properties using the implication and equivalence operators. Both operators are built using *AsmL's implies* operator.
- 3) *PSL Built Functions* include all functions defined by PSL to operate at the Boolean layer. We distinguish here two methods: a method that provides the previous values of a variable (e.g., *prev()*) and a method that provides the future values of a variable (e.g., *next()*). For both

methods, we define a queue structure that extends the *PrimitiveArray* class of AsmL, to store the values of the signals (*PSL_Bit_Vector_Queue* for the *PSLBitVector* type). We note that all methods over the Boolean layer are overridable according to the type of the input. This approach simplifies writing the properties in the ASM syntax as they will look very close to the PSL structure.

Figure 2 shows the AsmL code for the *PSL_Bit_Vector* class with the method *IsInitialized()* that checks if a BitVector is initialized.

```
class PSL_BitVector
  var m_size as Integer = 1
  var m_sum as Integer = 0
  var m_array as PrimitiveArray of PSL_Bit = null
  public IsInitialized() as Boolean
    non_initialized =
      (exists x in {1..m_size} where
        (m_array(x).m_value =
          X or m_array(x).m_value = Z))
    return not non_initialized
```

Fig. 2. ASM Embedding of PSL BitVector.

B. Temporal Layer

The most important part of this layer is the Sequential Extended Regular Expressions (SERE) feature, which embedding mainly includes:

- 1) *Sequential Expressions*, where a SERE is defined as an AsmL sequence of Boolean. It offers several operations to construct, manipulate and evaluate the SERE expression. *PSL_Sequence* extends the *PSL_SERE* class. It adds operations needed to create and update the SERE.
- 2) *Properties* in the form of operations necessary to create properties from sequential expressions. It also controls when and how the sequence is to be verified (i.e., the property “verify the sequence is true after n states” is defined as *PSL_Property.EvaluateNext(n)*).

Figure 3 shows the example of the *PSL_SERE.Evaluate()*, which checks if a sequence is true in a certain path. This method is activated according to an *INIT* signal that must be set by the property.

C. Verification Layer

This layer is intended to tell the verification tool how to perform the verification process. It allows the construction of assertions from properties and to specify relations between them. The embedding mainly includes:

- 1) *Verification Directives* to specify how the property will be interpreted (assertion, requirement, restriction or assumption). This class extends the *PSL_Property* class from the temporal layer.
- 2) *Verification Unit* is a compact way to include several properties together. The embedded class includes several operations to add/remove and update the unit’s list of properties.

```
class PSL_SERE
  var m_size as Integer = 0
  var m_seq as Seq of Boolean
  var m_actualState as Integer = 0
  var m_evaluation as SERE_Evaluation =
    NOT_STARTED
  var m_evaluationState as SERE_Evaluation =
    NOT_STARTED
  public Evaluate() as SERE_Evaluation
    require m_evaluationState = INIT
    if (me.m_seq(m_actualState) = false)
      m_evaluation := FAILED
      return FAILED
    else
      if m_actualState = m_size
        m_actualState := m_actualState + 1
        return IN_PROGRESS
      else
        m_actualState := 0
        return SUCCEEDED
```

Fig. 3. ASM Embedding of PSL SERE.

Figure 4 shows the *PSL_VerifLayerUnit.CopyFrom()* and *PSL_VerifLayerUnit.CopyTo()* methods. These latter are usually used to construct the unit by copying properties from or into other existent units, respectively.

```
class PSL_VerificationLayerUnit
  var m_name as String = ""
  var m_size as Integer = 0
  var S as Seq of PSL_FL_Property = null
  CopyFrom(vunit as PSL_VerificationLayerUnit)
    forall i in {1..m_size}
      me.AddProperty(vunit.S(i))
  CopyTo(vunit as PSL_VerificationLayerUnit)
    forall i in {1..m_size}
      vunit.AddProperty(me.S(i))
```

Fig. 4. Embedding of the PSL Verification Layer in ASM.

D. Modeling layer

This layer is not used in our verification approach since it is intended for VHDL and Verilog flavors of PSL. So we did not consider it in our current embedding.

PSL properties are embedded in ASM as assertions, the assertion here means the validity of the property and provides a unique view of the property in every system’s state. It also simulates the design with the property as a monitor. We build the assertion starting from basic Boolean components, sequences, and then verification units. We encapsulate sequences in the verification unit as an assertion that is embedded in the design. Given a set of Boolean items x_1, x_2, \dots, x_n , and y_1, y_2, \dots, y_m belonging to the Boolean layer, and the sequences, S_1 and S_2 belonging to the temporal layer, we can define: $S_1 = \{x_1, x_2, \dots, x_n\}$, and $S_2 = \{y_1, y_2, \dots, y_m\}$ and then use assertions to check any PSL operation between S_1 and S_2 such as $S_1 OP S_2$, where OP is a PSL operator (e.g., implication (\Rightarrow), or equivalence (\Leftrightarrow)). The assertion is built as follows:

1. Add all Boolean items to the sequences:

$$\forall i \text{ in } 1 \text{ to } n : S_1.AddElement(x_i)$$

$$\forall j \text{ in } 1 \text{ to } m : S_2.AddElement(y_j)$$

2. Create the property: $P := S_1 \text{ OP } S_2$
3. Define the *verification unit* as an assertion, say A , that includes the above property: $A.Add(P)$

This assertion will be embedded in every state in the FSM generated by the AsmL tool as a Boolean state variable, and therefore the FSM will include, by construction, a Boolean state variable giving the state of the property. Model checking tools, like SMV, can be used to check the correctness of the property on the generated FSM. The fact that we embed the property in the generated FSM provides a clear definition of the property, since its state variables are evaluated in every state by the AsmL tool, and the model checker just needs to perform reachability analysis on the model without the need to calculate the valuation of the property in every state. The final generated FSM is concrete and includes only Boolean variables to represent the state of the PSL properties. This will significantly reduce the verification time as will be illustrated in the case study discussed in the next Section.

IV. APPLICATION WITH SYSTEMC

In this section, we show an application to SystemC verification based on the proposed PSL embedding in ASM. SystemC [14] was introduced as a new system level language to overcome the problem of the growth in complexity and size of systems combining different types of components, including microprocessors, DSPs, memories, embedded software, etc. SystemC meets the need for a system level language that can fill the gap between hardware description languages (HDLs) and traditional software programming languages. SystemC comprises C++ class libraries and a simulation kernel used for creating behavioral and RTL designs. It can provide the common development environment needed to support software engineers working in C/C++ and hardware engineers working in HDLs such as Verilog or VHDL.

In order to apply PSL property checking on a design language, here SystemC, that language should also be embedded in ASM. In fact, the semantics of SystemC 2.0 using ASM were first defined by Müller *et. al.* [12]. However, fundamental features of SystemC 2.0 were not defined, including some SystemC primitive and hierarchical channels, design rules for SystemC channels, and most importantly the semantics of the SystemC simulator. An extended semantics of the SystemC simulator has been defined using ASM rules in [2] including a model for the SystemC simulator, the primary classes that are necessary to model SystemC designs and execute them, and the semantics of the main functions of the following components: SystemC signal, SystemC FIFO, SystemC mutual exclusive (MUTEX) channel, message queue, request-grant protocol, FIFO with handshake protocol [2].

The above embedding allowed us to translate SystemC designs into ASM models. Together with the PSL embedding described in this paper, we can generate a single model combining both the properties and the design model in one

single formalism, namely ASM. Details about the SystemC to AsmL and AsmL to SystemC transformations can be found in [8].

In order to illustrate the proposed verification methodology, we consider an extension of the Simple Bus Prototype Structure provided as part of the SystemC distribution [14]. It includes several SystemC components and shows the principles of using SystemC at the transactional level. Besides, some of the sample properties we checked, including liveness and safety, cannot be verified using simulation. They require the usage of formal techniques such as model checking.

A. Bus Description

Figure 5 shows the bus structure with N masters and M slaves. Each master is identified by a unique priority that is represented by an unsigned integer number. The lower this priority number is, the more important the master is. Each master communicates with the bus via an interface, which describes the communication between the masters and the bus. The slave interface describes the communication between the bus and the slaves. Multiple slaves can be connected to the bus. The slave returns an acknowledgment immediately upon receiving the data. The arbiter is responsible for choosing the appropriate master when there is more than one connected to the bus. It performs the selection according to the priority of the master. There are two possible modes for the bus: (1) *Blocking Mode*, where data is moved through the bus in a burst-mode. Here, the transaction cannot be interrupted by a request with a higher priority, (2) *Non-Blocking Mode*, where the master reads or writes a single data word.

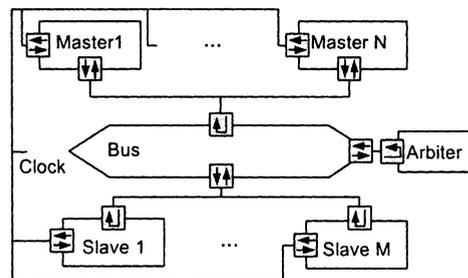


Fig. 5. Simple bus structure.

B. Bus Properties

For illustration purposes, we considered two properties for the bus architecture: one for the non-blocking master mode, and the other for the blocking master mode.

Property P1:

If ($(MasterBlock.Request = true) \ \& \ (BusStatus = OK) \ \& \ (MasterBlock.Priority \text{ is the highest})$) *then*
 $(MasterBlock[3] = OKSend) \ \& \ (BusStatus[3] = Used) \ \& \ (MasterBlock.DestSlave[4] = Recev) \ \& \ (MasterBlock.DestSlave[5] = Ack) \ \& \ (MasterBlock[7] = Done) \ \& \ (Bus[8] = Ready)$

meaning that when a blocking master generates a request while it has the highest priority to use the bus and the bus is

available, then at the third clock cycle, the status of the master should be *OKSend*, and the bus should be in the *Used* status. Then the status of the destination slave should be *Recev* at clock cycle 4, and *Ack* at clock cycle 5. The status of the master should be *Done* at clock cycle 7, and finally the bus becomes ready to handle new requests (i.e., bus status set to *Ready*) at clock cycle 8.

Property P2:

If ((MasterNBlock.Request = true) & (BusStatus = OK) & (MasterNBlock.Priority is the highest)) *then* (MasterNBlock[3] = OKSend) & (BusStatus[3] = Used) & (MasterNBlock.DestSlave[4] = Recev) & (MasterBlock[5] = Done) & (Bus[5] = Ready)

P2 can be interpreted in a similar way as property P1.

Both properties were defined in AsmL based on the embedding of the PSL layers. Figure 6 shows, as an example, the definition of P1. The property is included in a PSL unit as an implication of two sequences seq1 and seq2, which are formed from basic Boolean items (Bi1()) and Bi2() for seq1 and Bi3() through Bi7() for seq2. The construction of the above unit includes four steps:

- Creating the basic Boolean items: Bi1() to Bi7().
- Creating the sequences: seq1 and seq2.
- Constructing the implication property (P1) from seq1 and seq2 using the implication operator.
- Putting P1 into an embedded PSL unit.

C. Experimental Results

For experimental purposes, we generated FSMs for different combinations of the number of masters and slaves in order to evaluate the generation algorithm used inside the AsmL tool, and to illustrate the efficiency of our methodology. In every state, we include the evaluation of the property P1 that will be used by the model checker. P1 can take any of these five states: *NotStarted* (the required conditions to evaluate the property are not satisfied yet), *Started* (all the required conditions to start evaluating the property are satisfied), *Evaluating* (the evaluation of the property is in progress and no error is found), *FALSE* (the property is found to be false in this state) and *TRUE* (the property is true at this state). The property in SMV is defined as:

Property1:

assert (not (P1_Status = FALSE) and (P1_Status = Started) => F(P1_Status = TRUE)).

The machine time (user time) needed for generating the state machine depends on the complexity of the original model as well as the size of the generated state machine. Figure 7 displays the user time and number of transition for different combinations of the number of slaves and masters operating on the bus for generating the FSM model and PSL property. For example, for four slaves and eight masters, there were 4630 transitions, and it took around half an hour to generate the state machine. The experiments were conducted on a Pentium IV processor (2.4 GHz) with 256 MB of memory.

The above experimental results show that the number of transitions and machine time grow exponentially with the

```

var masterB1 as C_MasterBlocking =
    new C_MasterBlocking
var masterB2 as C_MasterBlocking =
    new C_MasterBlocking
MASTERSB = {masterB1, masterB2}
Bi1() as Boolean Bi: Boolean Item
    return exists master in MASTERSB where
        master.m_status = MasterReq
Bi2() as Boolean
    return exists master in MASTERSB where
        master.m_Priority = max y |
            y in {MasterReq.m_Priority}
Bi3() as Boolean
    return master.m_status = MasterOKSend
Bi4() as Boolean
    return exists slave in SLAVES where
        slave.ID = master.m_Destination and
        slave.m_Status = SlaveReceive
Bi5() as Boolean
    return exists slave in SLAVES where
        slave.ID = master.m_Destination and
        slave.m_Status = SlaveAck
Bi6() as Boolean
    return master.m_status = MasterReady
Bi7() as Boolean
    return bus.m_status = BusOK

var seq1 as PSL_SERE = PSL_SERE(2)
    seq1.AddElement(param1, param2)
var seq2 as PSL_SERE = PSL_SERE(5)
    seq2.AddElement(Bi2, Bi3, Bi4, Bi5, Bi6, Bi7)
var property as
    PSL_FL_Property = PSL_FL_Property()

property.AddImplication(seq1, seq2)
var Assertion1 as PSL_VerificationLayerUnit =
    new PSL_VerificationLayerUnit('Assertion1')
Assertion1.AddProperty(property)
    
```

Fig. 6. Definition of the PSL Property P1 in AsmL.

number of operating masters. Therefore, the AsmL tool could not handle more complex combinations like seven masters with four slaves and so failed to generate the state machine. This is because of the limitations of the algorithm used inside the AsmL tool.

The AsmL tool provides the option to generate the FSM in the dot format. We translated this representation into SMV code and conducted model checking using the SMV tool. Figure 8 provides the verification results of the above properties for the same set of combinations of masters and slaves. Accordingly, the PSL properties were found correct in less than 30 sec., even for the most complex cases. Therefore, we believe any improvement in the approach will come at the level of improving the generation of the FSM from the ASM code. In this paper, we used the algorithm implemented in the AsmL tool as a black-box. We will consider in a future work the introduction of new algorithms that will take advantage of both the SystemC system level design particularities and the property content and structure as defined in PSL.

V. CONCLUSION

In this paper, we presented an embedding of the Property Specification Language (PSL) in Abstract State Machines (ASM). We provided a deep embedding in ASM of the three

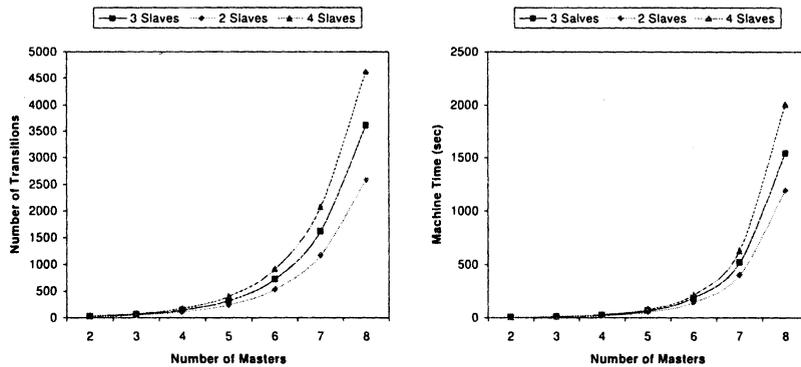


Fig. 7. FSM generation results for the bus model and the PSL properties.

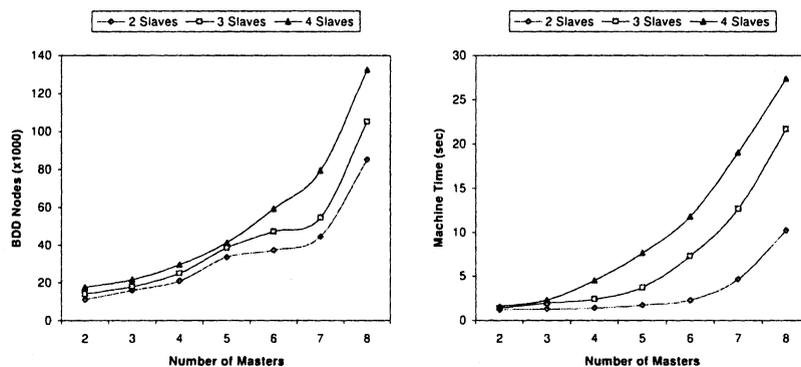


Fig. 8. SMV model checking results for the bus model and the PSL properties.

hierarchical layers: Boolean, temporal, and verification of PSL. An ASM model combining both the reduced design and the PSL property is input to the AsmL tool, which compiles it into C#, and generates its FSM. The verification of PSL properties is performed using the SMV model checker after translating the FSM model (given in *dot* format) into the input language of SMV.

We used a previously defined embedding of the semantics of SystemC components library and simulator in order to achieve the verification of PSL properties on SystemC designs. We illustrated this approach through the case study of a bus structure model, on which we verified several PSL sample properties for a system including up to eight masters and four slaves. This was not possible by directly verifying the PSL properties on the original SystemC design model using any of the publicly available tools. As future work, we plan to improve the proposed algorithm to generate more efficient FSMs that take into consideration the property under verification. Furthermore, we intend to evaluate the verification of PSL assertions by simulation using the interface offered by the AsmL tool to the .NET framework.

REFERENCES

- [1] K. Claessen and J. Martensson. An Operational Semantics for Weak PSL. In *Formal Methods in Computer-Aided Design*, LNCS 3312, pages 337–351, Springer-Verlag, 2004.
- [2] A. Gawanmeh, A. Habibi and S. Tahar. Enabling SystemC Verification using Abstract State Machines, Proc. Languages for Formal Specification and Verification, Forum on Specification & Design Languages, Lille, France, September 2004.
- [3] W. Grieskamp, Y. Gurevich, W. Schulte, and M. Veanes. Generating Finite State Machines from Abstract State Machines. *Software Engineering Notes*, 27(4):112–122, 2002.
- [4] M. Gordon, J. Hurd and K. Slind. Executing the formal semantics of the Accellera Property Specification Language by mechanised theorem proving. In *Correct Hardware Design and Verification Methods*, LNCS 2860, pages 200–215. Springer-Verlag, October 2003.
- [5] M. Gordon and T. Melham. *Introduction to HOL: A Theorem Proving Environment for Higher-Order Logic*, Cambridge, U.K., Cambridge University Press, 1993.
- [6] M. Gordon. Validating the PSL/Sugar Semantics Using Automated Reasoning. *Formal Aspects of Computing*, 15(4):406–421, 2003.
- [7] Y. Gurevich. *Evolving Algebras 1995: Lipari Guide*. In *Specification and Validation Methods*, Oxford University Press, 1995.
- [8] A. Habibi and S. Tahar. On the Transformation of SystemC to AsmL using Abstract Interpretation; *Electronic Notes in Theoretical Computer Science*, 131: 39–49, 2005.
- [9] J. Huggins. Abstract State Machines website. <http://www.eecs.umich.edu/gasm>, 2006.
- [10] M.L. McMillan. *Symbolic Model Checking*, Kluwer Academic Pub., 1993.
- [11] AsmL for Microsoft .NET (version 2.1.5.7), Microsoft. <http://www.research.microsoft.com/foundations/asml>, 2003.
- [12] W. Müller, J. Ruf, and W. Rosenstiel. *SystemC Methodologies and Applications*. Kluwer Academic Pub., 2003.
- [13] Accellera Property Specification Language Reference Manual, Version 1.1. <http://www.accelera.org>, 2006.
- [14] SystemC. <http://www.systemc.org>, 2006.
- [15] C. Wallace. *The Semantics of the C++ Programming Language*. In *Specification and Validation Methods*, Oxford University Press, 1995, pages: 131–164.