

A Framework for the Verification of SystemC Transaction Level Models

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Revolutionary new system specification languages which build on recent advances in microelectronics system-form processors, memory and advanced operating system through to sensors and networking- can now be integrated into a single chip, known as System-on-Chip (SoC). SoC technology requires a design language, or System Level Language, which can model both the software and the hardware. In this respect, SystemC [7] is regarded as one of the most relevant system level modeling and simulation languages that has become an industry standard, adopted by more than twenty thousand users. However, the language is in its infancy and still has great need for good verification tools and techniques.

We propose a framework for the verification of system level designs modeled in SystemC. It includes a static analysis module to abstract SystemC designs; hence, reducing their complexity for better model checking and assertion based verification performance. The static analysis is based on abstract interpretation techniques, which can handle large and complex systems. Furthermore, it enables the static verification of critical problems such as infinite loops. In our static analysis environment, we provide a graphical environment offering interaction with the user for better analysis results. It also includes two views of the design under analysis (events environment and program environment) and a complete model of the memory. Hence, it also allows abstract debugging of the design [6].

For model checking, the reduced model is first translated to AsmL [2] (Abstract State Machines Language) and checked against properties written in PSL [1] (the Property Specification Language standard). AsmL is integrated with Microsoft's software development environment including Visual Studio, MSWord, and Component Object Model (COM). It enables a higher level of abstraction and provides an interface for multiple model checking and theorem proving tools such as SMV and PVS. Besides, using the AsmL tool from Microsoft, AsmL code can be compiled and translated to C# or connected to the .NET framework. Our model checking procedure generates the FSM (finite state machine) of the design, then in case of error, it produces a complete trace of the error starting from the initial state; otherwise a good guidance for test vectors generation is provided in case of successful verification [4].

We embedded the PSL language in AsmL [4], where the user defines directly the design properties in AsmL according to the PSL syntax. When the model checking does not terminate due to state explosion, we complete the verification process by enabling assertion based verification. For instance, the PSL assertions are compiled to generate a set of C# modules that are plugged in read-only mode to the SystemC design then verified by

simulation. Furthermore, we embedded a genetic algorithm to guide the test vectors generation in order to enhance the simulation coverage [6]. Early results of this approach when applied to a Master/Slave Bus structure from the SystemC library showed interesting results [4].

Our framework has shown promising results when applied to commercial standard designs such as the PCI bus [8], the look-aside interface [5], and the AGP bus. Its performance has been compared to other commercial tools such as RuleBase from IBM and FormalCheck from Cadence.

Figure 1 displays a diagram providing details about the overall SystemC verification framework described above and tagged *SC-Verifier*. More details are available at: <http://hvg.ece.concordia.ca/Research/SoC>.

References

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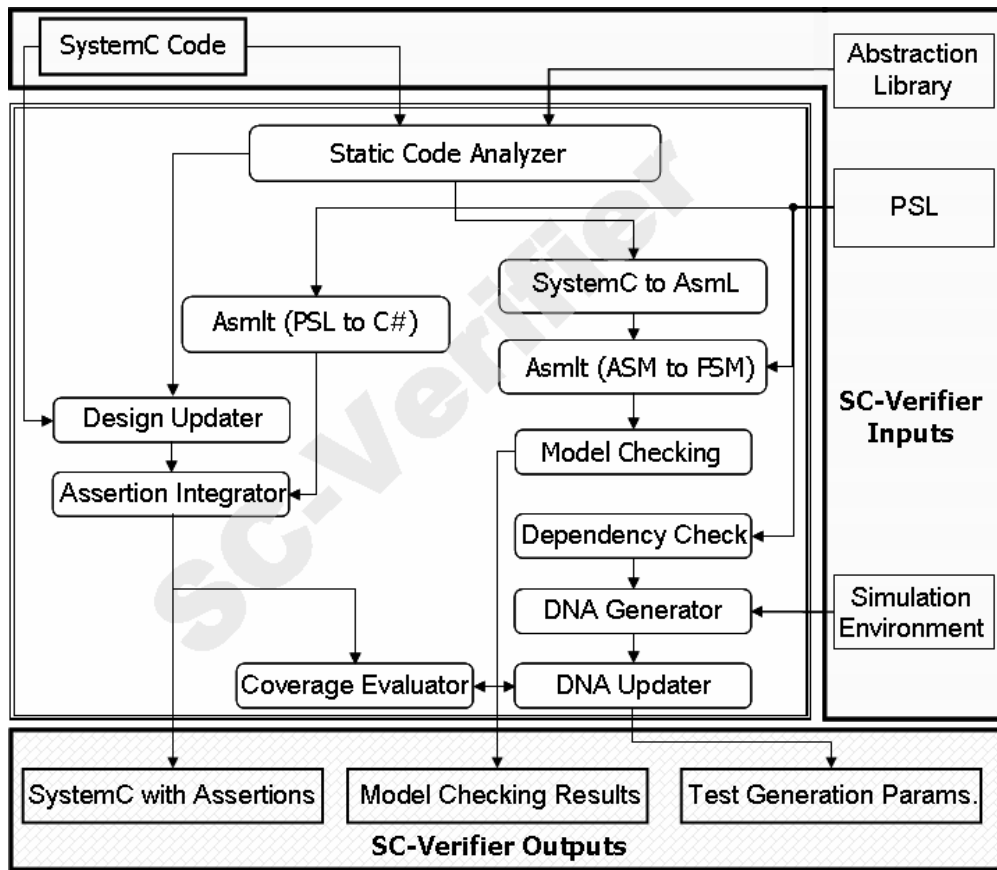


Figure 1. SC-Verifier: SystemC Verification Framework