Using Pattern Matching for Ensuring Correctness of Oscillator Start-Up Condition

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Oscillators [3] [4] are critical components in any analog designs for which researchers in the last decade have come up with new simulation (monitors) [1] and formal [2] based methodologies for their property verification. In the current state of the art, monitors can only check for certain functions of the circuit like voltages threshold crossing at a certain node or current bounds on a certain path of the circuit. That leaves most of the circuit behavior unchecked as in the case of checking abnormalities during transient response of the circuit. Conversely, success in formal techniques has been mainly limited by scalability issues due to the complexity of generating formal models and the computational overhead of the algorithms.

This paper tries to address some of the shortcoming of the above approaches, by using pattern matching for ensuring the correctness of oscillator *start-up condition*. For instance, given an oscillator circuit that has been simulated by *N* different designers across different design centers, generating *N* different outputs under different process variation conditions, we address the question of "*how to decide on the acceptance/rejection of those circuits based on start-up condition?*"

The Longest Common Subsequence (LCS) is a pattern matching algorithm that finds its applications in computational biology, chip layout design, etc. As opposed to the traditional approach of comparing the output of the design to its specification value, we can extend the LCS algorithm to estimate, in terms of percentage, the exact (100%) or *"closely"* matched simulated output relative to the ideal circuit output. The idea is to find the *longest closest subsequence* (LCSS) [6] from a set of non-ideal sequences in order to determine circuits that start-up in shorter time. By doing so, instead of blindly rejecting the circuit that violates the specification, designers will have more information during the evaluation and hence can make viable decisions.

Figure 1 shows the overall verification methodology based on the LCSS algorithm. For process variation, technology vendors create a library of devices with different corners that characterize the device in terms of power, speed, area, etc. This allows the designers to choose from a range of devices based on the application. Thereafter, the analog design described as a netlist, along with process variation, and the environment constraints is evaluated using Monte Carlo simulation. Based on the number of Monte Carlo trials, we generate sets of sequences, one considered to be the sequence of an ideal circuit and the rest of the sequences representing non-ideal circuits due to process variation. These sequences along with the given tolerance level (p) are evaluated using the start-up and LCSS algorithm as shown in Figure 1 in order to generate the percentage of matched sequence.

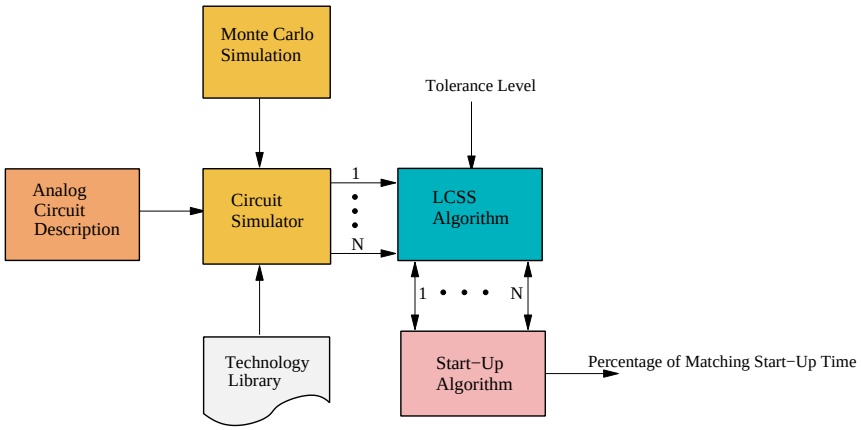


Figure 1: Overall Methodology

Given two sequences of analog circuit output values $X = \{X_1, X_2, \ldots X_m\}$ and $Y = \{Y_1, Y_2, \ldots Y_n\}$, then for a given tolerance level *p*, $\exists Z = \{Z_1, Z_2, \ldots Z_k\}$, an increasing maximum-length common subsequence, if Z is a subsequence of both X and Y. Here, we choose X to be the output sequence of an ideal circuit and Y is the output of the non-ideal circuit as described in the following property [6]:

Let $X = \{X_1, X_2, \ldots X_n\}$ and $Y = \{Y_1, Y_2, \ldots Y_m\}$ be sequences, and let $Z = \{Z_1, Z_2, \ldots Z_k\}$ be any LCSS of X and Y. Then, for a given tolerance level p,

(1) If $Y_n \leq (X_m$+p) and $Y_n \geq (X_m$-p), then Z_k is an LCSS of X_m and Y_n.

(2) If $X_m \neq Y_n$, then $Z_k \neq X_m$, then Z is an LCSS of X_{m-1} and Y.

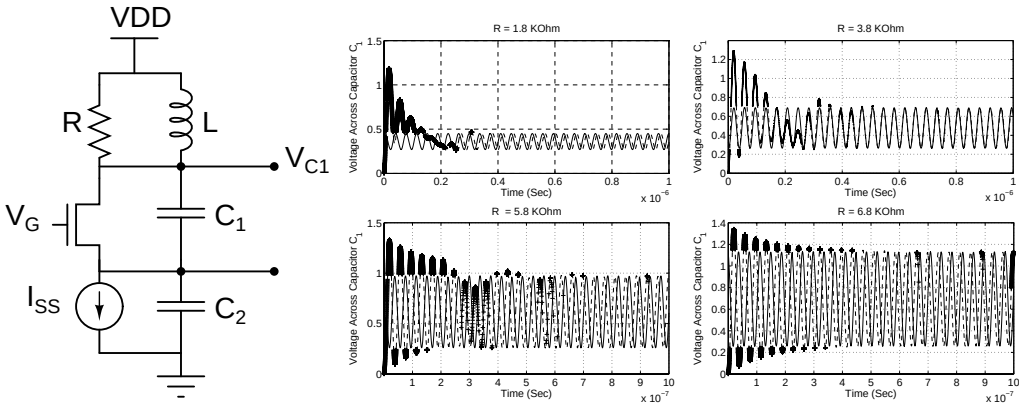
(3) If $X_m \neq Y_n$, then $Z_k \neq Y_n$, then Z is an LCSS of X and Y_{n-1}.

In general, the start-up condition that represents the time can be considered as a horizontal offset of the signal as described in the following algorithm, where in order to determine the start-up time, it is necessary to first find and eliminate any vertical offset in the signal. The first step is to determine the frequency of the signal. Then, we derive the period of the signal and divide those sequence length by the period in order to calculate the minimum and the maximum of each period (line 3). This is followed by vertical offset elimination (lines 4-7). We then apply the LCSS algorithm to determine the pattern matching between the ideal signal and the non-ideal signal. If the non-ideal signal matches from its first values, we can consider that to be the start-up condition (lines 8-9).

Algorithm 1 Start-Up Algorithm

Require: X, Y, p
1: $M \leftarrow Length[X]$
2: $N \leftarrow Length[Y]$
3: $number\_of\_periods \leftarrow Period(N, Y)$
4: **for** $i \leftarrow 1$ *to* $number\_of\_periods$ **do**
5: $\quad Vertical\_Offset \leftarrow Offset\ Estimation\_for\_each\_period$
6: **end for**
7: $Y \leftarrow Y - Vertical\_Offset$
8: $[percentage\_of\_matching, deleted\_values] \leftarrow LCSS(X, Y, p)$
9: $StartUp\,Time \leftarrow decision(deleted\_values)$

We applied the proposed approach on a Colpitts oscillator circuit in a MATLAB simulation environment[1]. For the correct choice of component values, the circuit will oscillate due to the bias current and negative resistance of the passive tank. The frequency of oscillation is determined by L, C_1 and C_2 as shown in Figure 2 (a).



(a) Colpitts Oscillator Circuit (b) Colpitts Start-Up Condition

Resistor Ω	Start-Up Time (Sec)
1800	3.09e-7
2800	4.6e-7
3800	5.12e-7
4800	5.0e-7
5800	7.0e-7
6800	4.3e-7

(c) Start-Up Time Results

Figure 2: Colpitts Simulation

Figure 2 (b) shows the simulation results. For demonstration purposes, we have chosen the process variation on the resistor *R* only. The bold traces show the derivation of the start-up time for the non-ideal sequence (dotted line) with respect to the ideal sequence (black line). Table summarizes the start-up time derivation for different resistor values which concludes that *R = 1800* Ω provides the shortest start-up time

References

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[1]Currently, we are working towards the CADENCE circuit simulation environment.