# Generation of Reduced Analog Circuit Models using Transient Simulation Traces

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## ABSTRACT

The generation of fast models for device level circuit descriptions is a very active area of research. Model order reduction is an attractive technique for dynamical models size reduction. In this paper, we propose an approach based on clustering, curve-fitting, linearization and Krylov space projection to build reduced models for nonlinear analog circuits. We demonstrate our model order reduction method for three nonlinear circuits: a voltage controlled oscillator, an operational amplifier and a digital frequency divider. Our experimental results show that the reduced models lead to an improvement in simulation speed while guaranteeing the representation of the behavior of the original circuit design.

## Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids—*Simulation*

## Keywords

Analog Circuits; Curve-Fitting; Model Order Reduction; Krylov Space

## 1. INTRODUCTION

Device level simulation is a main step to validate electronic circuits before their fabrication. This step became very computationally expensive because of the large size and nonlinearity of their models. Therefore, researchers are looking for methods to build faster circuit models which preserve the same device level accuracy. Such models are needed to fasten simulation and enhance verification methodologies. Model abstraction, simplification and linearization are methods to deal with the complexity of large dynamical models. However, for the case of analog circuits they can lead to inaccurate models which do not preserve their characteristic nonlinear behaviour. Model Order Reduction (MOR) [1] is an attractive technique which consists in transforming a mathematical circuit model into a macromodel using a well defined algorithm. The resulting reduced model simulates in much smaller time than the full order model while reproducing the same behaviour. The most promising MOR algorithms for the reduction of analog circuits are the Trajectory Piece-Wise Linear MOR method (TPWL) [13], the General-Purpose Nonlinear MOR using Piecewise-Polynomial Representations [7] and the MOR method for nonlinear circuits based on state space clustering [2]. These methods employ Taylor expansions representations and Krylov space projection to reduce dynamical circuit model in the form of Ordinary Differential Equations (ODEs).

Curve-fitting is a very powerful method used in different scientific areas to construct models from a series of data points [12]. It is a very effective approach especially for partially known models. This is the case of analog circuit models generated through Modified Nodal Analysis (MNA), when their semiconductor devices I-V characteristics are not completely specified or are missing some parameters [6].

In this paper, we propose an automated approach to build reduced models for nonlinear analog circuits, based on curve-fitting, clustering, linearization and MOR via Krylov space projection. Parametric nonlinear models are built via MNA and are curve-fitted using SPICE circuit simulation traces to obtain accurate nonlinear dynamical models. Then, linearization and state space reduction via Krylov space projection are applied at different state space clusters to obtain circuit reduced models.

In what follows, the related work is briefly reviewed in Section 2. Then, Section 3 details our method to generate circuit reduced models using their netlist and simulation traces. After that, our experimental results are shown in Section 4 for three nonlinear circuits: a voltage controlled oscillator, an operational amplifier and a frequency divider. Finally, our conclusions and future work are presented in Section 5.

## 2. RELATED WORK

In the last two decades many researchers realized the possibilities offered by MOR and tried to improve and apply these methods. There have been different successful methods to approximate transfer functions of linear circuits like the Singular Value Decomposition (SVD) and the Krylov Space projection methods [1]. However, for the case of nonlinear circuits, MOR methods are still in development phase. The Proper Orthogonal Decomposition (POD) that is the adaptation of the SVD method for nonlinear models is being used to reduce Partial Differential models successfully [1]. For the case of weakly nonlinear circuits, a MOR based on approximating nonlinear terms with quadratic Taylor ap-


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proximations and Krylov space projections is proposed in [4]. Also, the TPWL MOR, based on linear Taylor approximations, was applied to nonlinear transmission lines, amplifier chains and Micro-machined devices [13]. The general purpose MOR method, based on piecewise polynomial representations [7], and the MOR method, based on state space clustering [2], improve the TPWL by addressing the problem of input dependency. Recently, three different MOR methods called ManiMOR, QLMOR and NTIM were proposed to derive reduced models for circuits and biology models [8]. Their accuracy is enhanced by using nonlinear manifolds projection, canonical representation and Volterra analysis. However, the resulting reduced models are intended for a specific type of analysis: DC, AC responses and timing/phase responses.

Curve-fitting is an inverse-problem where the objective is to determine parameters of a candidate model given a desired system response. For analog circuits, curve-fitting was used to determine a power MOSFET model parameters using experimental results [3]. Also, a piecewise curve-fitting modelling technique was proposed to determine accurate low order impedance transfer functions for capacitors and inductors from experimental data [11]. Recently, a method for parametric fault detection based on polynomial curve-fitting was applied to the case of a biquad filter [10]. However, none of these approaches can be used to curve-fit a large size analog circuit model.

In this paper, we are rather interested in determining dynamical model parameters for large analog circuits using a nonlinear curve-fitting constrained to a minimum mean squared error and reducing these models using a projection type MOR approach.

# 3. MOR METHODOLOGY

The proposed methodology for the generation of reduced models of large analog circuits using their transient simulation traces and their netlist is depicted in Figure 1. We apply first MNA to elaborate a mathematical model for the given circuit netlist, after replacing each active device with an equivalent circuit. The I-V-characteristic parameters of each equivalent circuit are unknown which leads to a parametric nonlinear differential model describing the circuit dynamics. Then, we use curve-fitting to extract the missing parameters from the circuit simulation traces performed in SPICE. The obtained circuit model is validated through simulation and comparison with the original simulation traces. In parallel, we perform clustering of the simulation traces in order to select linearization points which will be used for a piecewise linear description of the nonlinear differential model obtained via curve-fitting. After that, we compute a Krylov space projection matrix using the Arnoldi algorithm and reduce the local linearized models via projection, as described in [2]. Finally, the obtained reduced model is validated against the original nonlinear model within a testbench. We simulate the reduced model for different inputs and conditions and check its accuracy, input sensitivity and speedup.

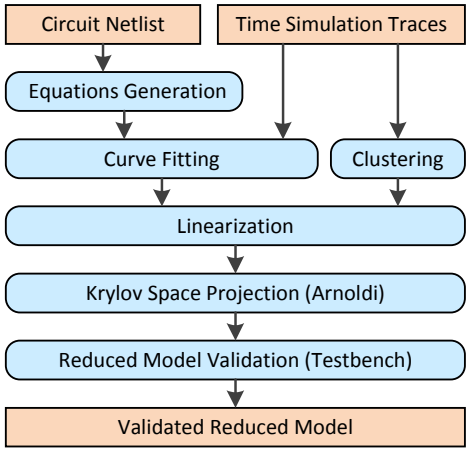


**Figure 1: Model Order Reduction Methodology**

## 3.1 Equations Generation

In order to perform an accurate curve-fitting, the generation of a good function guess is essential. In fact, the function guess must be capable of reproducing the main transient characteristics of the active devices. Semiconductor devices can include hundreds of parameters. In our approach, these elements are modeled using basic transient equivalent circuits consisting mainly of Voltage Controlled Current Sources (VCCS) and possibly some constant parasitic capacitances and resistances. The VCCS models are piecewise defined functions with linear and quadratic terms for MOSFETs and exponential terms for diodes and BJTs. The parameters of these models have to be determined using curve-fitting. The replacement of the active elements leads to a circuit consisting only of the following two-port elements: capacitances, resistances, inductances, independent voltage and current sources and VCCS. The input voltages and currents as well as the passive elements models are extracted from the netlist. Having a two port elements equivalent circuit, we extract the differential model using the MNA formulation.

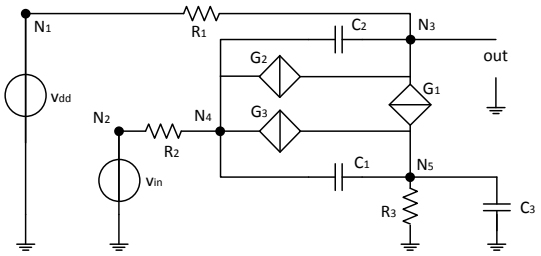


**Figure 2: One-BJT Amplifier Circuit with VCCS**

We demonstrate the equation generation step on a single BJT amplifier circuit, shown in Figure 2. The BJT element was replaced by its transient equivalent circuit and the MNA formulations leads to the set of matrices, shown in Equation (1).

$$\begin{aligned} C &= A_C \cdot C_0 \cdot A_C^T \\ G &= A_R \cdot R^{-1} \cdot A_R^T \end{aligned} \quad (1)$$

$$R=\begin{bmatrix}R_1 & 0 & 0\\ 0 & R_2 & 0\\ 0 & 0 & R_3\end{bmatrix}\ C_0=\begin{bmatrix}C_1 & 0 & 0\\ 0 & C_2 & 0\\ 0 & 0 & C_3\end{bmatrix}\ I=\begin{bmatrix}G_1\\ G_2\\ G_3\end{bmatrix}\ V=\begin{bmatrix}v_{dd}\\ v_{in}\end{bmatrix}$$

$$A_R=\begin{bmatrix}1 & 0 & 0\\ 0 & 1 & 0\\ -1 & 0 & 0\\ 0 & -1 & 0\\ 0 & 0 & 1\end{bmatrix}\ A_C=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & 0\\ 0 & -1 & 0\\ 1 & 1 & 0\\ -1 & 0 & 1\end{bmatrix}\ A_I=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & 0\\ 1 & -1 & 0\\ 0 & 1 & 1\\ -1 & 0 & -1\end{bmatrix}$$

- The resistance, capacitance and inductance matrices R, C, L are ordered diagonal matrices.
- Dependent and independent current and voltage sources are merged to the row vectors $I$ and $V$, respectively.
- The incidence matrices for all elements $A_R$, $A_L$, $A_C$, $A_I$ and $A_V$ are built based on their nodes information.

The matrices $C$ and $G$ are reduced to $C_{cut}$ and $G_{cut}$ by removing the lines related to the supply and input voltages, which are not considered as state variables. Then, the differential model is formed as given in Equation (2).

$$\dot{e} = C_{cut}^{-1} \cdot \left(-G_{cut} \cdot \begin{bmatrix}V\\ e\end{bmatrix} - A_I \cdot I(e,c)\right) \tag{2}$$

where $e = [v_{N_1}, v_{N_2}, v_{N_3}]^T$ is the state variables vector and $I(e,c)$ are the parametric VCCS models which depend on the state variables and the undefined parameters $c$. The matrix $C_{cut}$ has to be nonsingular to generate an ODE system and avoid a DAE system, which is not always solvable. For this purpose, very small parasitic elements can be considered, as $C_3$ in Figure 2. If the circuit contains inductances, their currents have to be added as state variables to Equation (2), which leads to one system of Equation (3).

$$\begin{aligned}\dot{e} &= C_{cut}^{-1} \cdot \left(-G_{cut} \cdot \begin{bmatrix}V\\ e\end{bmatrix} - A_I \cdot I(e,c) - A_L \cdot i_L\right)\\ \dot{i}_L &= L^{-1} \cdot A_L^T \cdot \begin{bmatrix}V\\ e\end{bmatrix}\end{aligned} \tag{3}$$

The general form of the differential model is given in Equation (4).

$$\dot{x} = f(x, c, u(t)) \tag{4}$$

## 3.2 Curve-Fitting

The curve-fitting step is performed as detailed in Figure 3. It requires the circuit transient simulation traces (state variables snapshots) and a function guess $f$ which is the incomplete circuit model given in Equation (4). After that, we approximate the state variables derivatives by finite differences approximation $\dot{x} \approx (\frac{\Delta x}{\Delta t})_s$ for different time samples $s$. The approximated state variables time derivatives provides a set of valuations of the function guess $f$. Then, the best-fit model parameters $c_{opt}$ are determined automatically using the Levenberg-Marquardt curve-fitting method [12]. It is also called the least-squares curve-fitting algorithm since it determine local best-fit parameters which minimize the least-square residual between the function guess values and the approximated time derivative, as shown in Equation (5).

$$c_{opt} = \min_c \|f(x_s, c, u_s) - (\frac{\Delta x}{\Delta t})_s\|_2 \tag{5}$$

The accuracy of the curve-fitting algorithm depends on the function guess choice, the approximated state variables time derivatives and the initial parameters guess $c_{init}$. Because of that, we solve numerically the differential model in Equation (4) with the obtained best-fit parameters and compare

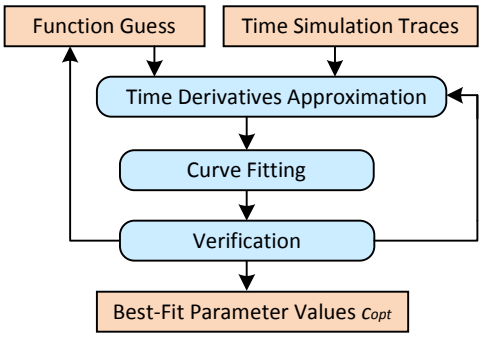


**Figure 3: Curve-Fitting Model Parameters**

the result with the time simulation traces. If the model is accurate, we proceed to the model reduction step. Otherwise, we add more training points $x_s$ which leads to the maximum error values, during the verification step. At the end, if the previous test did not improve the accuracy of the models, we change the initial function guess. In fact, the use of a proper function guess is necessary for a successful curve-fitting of the nonlinear behavior of analog circuits. For that reason, we use device models similar to the SPICE model but with a smaller set of parameters. Using only polynomial function guess, as the Vandermodes interpolation method [9], we do not get best fit-parameter set which can reproduce the large signal transient behaviour of the circuit devices. The reason is that some device I-V characteristics have piecewise exponential functions with different parameters and coefficients. Piecewise local interpolation also fails to approximate the states behavior as it leads to a linear dependent system of equations which does not have a unique solution. Using the described curve-fitting approach, we determine the complete differential model given in Equation (6).

$$\dot{x} = f(x, u(t)) \tag{6}$$

## 3.3 Linearization and Krylov Space Transformation

We select $k$ linearization points via Kmeans clustering of the simulation traces [12] and linearize the differential model in Equation (6), as detailed in [2, 13]. This leads to $k$ local linear models as given in Equation (7).

$$\dot{x} = f(x_l, u_l) + J_{x_l} \cdot (x - x_l) + J_{u_l} \cdot (u - u_l) \tag{7}$$

where the Jacobian $J_{x_l} = \frac{\partial f}{\partial x}(x_l)$ and $J_{u_l} = \frac{\partial f}{\partial u}(u_l)$ are computed numerically for each cluster $(x_l, u_l)$, using the Romberg extrapolation [5]. The piecewise weighted sum of the previous few local models is a good approximate of the differential model in $\mathbb{R}^n$. This intermediate model is reduced via Krylov space projection to get a smaller size differential model in $\mathbb{R}^m$, $m < n$, as given in Equation (8). A local $n \times m$ orthogonal projection matrix, which is necessary to do such a transformation, is computed using the Arnoldi algorithm [14]. Then, the main singular vectors of these local matrices form the unified projection matrix $U$. The reduced differential model is given in Equation (8).

$$\dot{z} = R_l + A_l \cdot (z - z_l) + B_l \cdot (u - u_l) \tag{8}$$

where $R_l = U^T \cdot f(x_l, u_l)$, $A_l = U^T \cdot J_{x_l} \cdot U$, $B_l = U^T \cdot J_{u_l}$ and $\vec{z}$ is the reduced state space vector that can be projected

back to the original state space to approximate the original full order state variable $x$ using the relation $\hat{x} = U \cdot z$. During the numerical simulation of Equation (8), the closest cluster $z_l = U^T \cdot x_l$ to the current state $z$ is determined and the local model around it is evaluated in order to determine the next state.

## 3.4 Reduced Model Validation

The reduced model must fit some requirements to be usable in practice. Its simulation time must be smaller than the simulation time of the original model. It has also to preserve the input-output behavior and be accurate for a range of input signals. We use a testbench environment to automatically check the generated reduced models and compare them to the original model simulations. For our applications, we measure the closeness of the reduced simulation output vector $\widehat{x}_o(t)$ and the original simulation output vector $x_o(t)$ with Equation (9).

$$error = \frac{\sum_{i=1}^{nt} ||x_o(i) - \widehat{x}_o(i)||}{\sum_{i=1}^{k} ||x_o(i)||} \tag{9}$$

where $nt$ is the number of time sample points. If different sample times are used for $x_o$ and $\widehat{x}_o$, we interpolate $\widehat{x}_o$ at the time $i$ using the closest trajectory points. The simulation speedup can be affected by the numerical integration method. Therefore, we use the same backward differentiation algorithm for both the reduced and the original model version in MATLAB [12]. Note that we cannot force the solver to use the same internal steps as it affects the solution accuracy. Also, the determination of the closest linearization point, which is done at every time step, can be time consuming if the current state is compared to a large number $k$ of linearization points. Even though, we do not have the original SPICE circuit models coded in the MATLAB environment, we still can illustrate the speedup of the simulations of our generated reduced models using models expressed in the original state space using SPICE-like equivalent models for active devices.

# 4. APPLICATIONS

In this section, we apply the current method to a two-stage operational amplifier, a $90-nm$ $CMOS$ voltage controlled oscillator (VCO), and a frequency divider. We show that the simulations of the generated reduced models are faster than that of the original models, while the error due to the reduction, evaluated using Equation (9), is minimal. Equation (10), illustrates a two parameters VCCS equivalent model for an $NMOS$ transistor used during the equation generation step, for all applications. The set of parameters $c_{1,2}$ is determined during the curve-fitting step and $x$ and $y$ are the gate to source and the drain to source transistor terminals voltages which values are extracted from the simulation traces.

$$I_{FET} = \begin{cases} 0 \quad if \quad x < c_1 \\ c_2 \cdot 0.5 \cdot (x - c_1) \;\; if \; y > x - c_1 > 0 \\ c_2 \cdot y \cdot (x - c_1 - \frac{y}{2}) \;\; if \; y < x - c_1 \end{cases} \tag{10}$$

For each of the following applications, a table shows the mathematical model size of the original state space (Equation (2)) and the reduced state space (Equation (8)).

## 4.1 Two Stage Operational Amplifier

Operational Amplifiers (OA) are extensively used in analog circuits applications such as communications and signal conversion. We use the two stage OA, in Figure 4, as an application to prove the effectiveness of the proposed reduction method. Its bias current is provided by a constant current source built by an $NMOS$ transistor and a resistance. The open loop gain of this OA is of the order of $6.6 \cdot 10^5$ at $1MHz$ operating frequency.

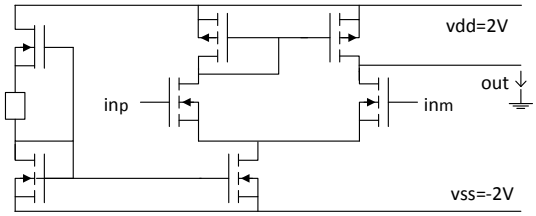


**Figure 4: Two Stage Operational Amplifier Circuit**

The number of best-fit parameters determined, during the curve-fitting step, is eight, as there are four different types of transistors in this circuit. The curve-fitted model have been validated against the original SPICE simulation traces. Table 1, gives the size of the original and reduced OA mathematical models. The reduced models 1 and 2 in rows 4 and 5 refer to the open loop OA and feedback loop OA configurations, respectively. The open loop OA configuration consists in grounding the negative input and connecting a sinusoidal input source to its positive input. The feedback loop OA configuration consists in connecting a resistance between the output node and the negative input which leads to a limited gain non-inverting OA.

**Table 1: Original and Reduced OA Sizes**

| Original | $C_{cut}^{-1}$ | $G_{cut}$ | $[V; e]$ | $A_I$ | $I(e)$ |
|---|---|---|---|---|---|
| | $30 \times 30$ | $30 \times 34$ | $34 \times 1$ | $30 \times 7$ | $7 \times 1$ |
| Reduced | $R_l$ | $A_l$ | $z$ | $B_l$ | $u$ |
| 1 | $27 \times 1$ | $27 \times 27$ | $27 \times 1$ | $27 \times 4$ | $4 \times 1$ |
| 2 | $25 \times 1$ | $25 \times 25$ | $25 \times 1$ | $25 \times 4$ | $4 \times 1$ |

The reduction of the feedback loop OA model needed 30 linearization points. However, we used 79 points for an accurate reduction of the open loop OA which can be explained by its very high gain and its strongly nonlinear behavior. This results in a much smaller speedup of the open loop OA as shown in row 2 of Table 2. Table 2, provides also in row 3 and 4 the results for the feedback loop reduced OA models simulations. In this configuration the reduced OA model is accurate and much faster that the OA original model.

**Table 2: OA Simulation Results for** $(in_p - in_m) = A \cdot \sin(2\pi \cdot f \cdot t)$

| A[V] | f[MHz] | Run Time[$s$] | | Speedup | Error |
|---|---|---|---|---|---|
| | | Original | Reduced | | $[10^{-2}]$ |
| $18\mu$ | 1 | 10.93 | 2.90 | 3.70 | 0.02 |
| $45m$ | 1 | 142.20 | 4.13 | 34.43 | 0.07 |
| $45m$ | 0.5 | 66.51 | 3.07 | 21.66 | 0.01 |

Figure 5 shows that the reduced and the curve-fitted OA models are accurate compared to the SPICE model.

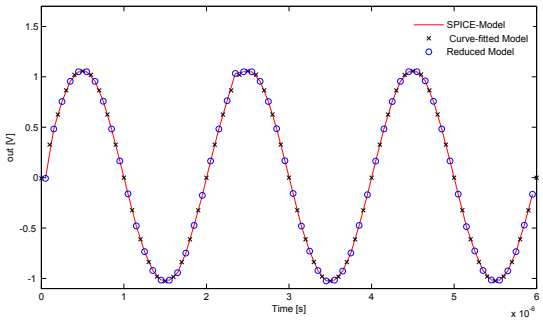


**Figure 5: Operational Amplifier Output Signal**

## 4.2 Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) is an ubiquitous circuit used for applications requiring an adaptive clock frequency, such as PLL. It generates a square output voltage with a frequency controlled by its input voltage. We applied our approach to the VCO given in Figure 6. It is implemented as a ring oscillator (central inverters chain $PMOS$ and $NMOS$ transistors) and a large current mirror (upper $PMOS$ and lower $NMOS$ transistors), which limits the current mirrored in each of the ring oscillator inverters. The curve-fitting of the VCO model requires 4 parameters

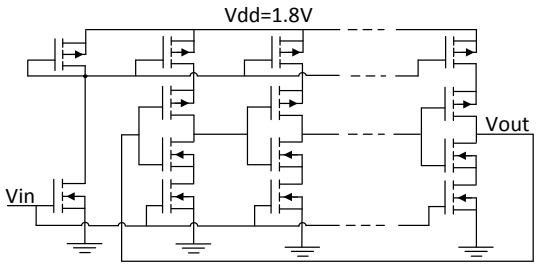


**Figure 6: Voltage Controlled oscillator Circuit**

for each of the equal size and same type transistors, leading to 16 parameters in total. The size of the original and reduced VCO models are given in Table 3. Table 4 reports the

**Table 3: Original and Reduced VCO Sizes**

| | | | | | |
|---|---|---|---|---|---|
| Original | $C_{cut}^{-1}$ | $G_{cut}$ | $[V;e]$ | $A_I$ | $I(e)$ |
| | $48 \times 48$ | $48 \times 50$ | $50 \times 1$ | $48 \times 62$ | $62 \times 1$ |
| Reduced | $R_l$ | $A_l$ | $z$ | $B_l$ | $u$ |
| | $33 \times 1$ | $33 \times 33$ | $33 \times 1$ | $33 \times 2$ | $2 \times 1$ |

different simulations results of the generated reduced VCO model. The reduced VCO model runs 5 times faster than the original VCO model for a reduction of the state variable size from 48 to 33. Reducing further the VCO leads to higher speedup values but requires also an adjusting of the set of linearization points. In all experiments, the accuracy of the reduced VCO model is good compared to the VCO original model. The last row of Table 4 shows also that the reduced VCO model is able to increase its output signal frequency after a step increase in its input frequency. This feature has been enabled because of the input dependent terms, in Equation (8), which makes the reduced models sensitive to small input variations. Figure 7 illustrates the output voltages behavior of the reduced VCO model, the curve-fitted model and the SPICE model. It shows that the three models are oscillating at the same frequency for the specified input voltage. The slight deviation from the SPICE simulation traces is mainly due to the accuracy of the curve-fitting step which uses different active device models than that of SPICE.

**Table 4: VCO Simulation Results**

| Input $Vin[V]$ | Run Time$[s]$ | | Speedup | Error $[10^{-2}]$ |
|---|---|---|---|---|
| | Original | Reduced | | |
| 1.2 | 21.75 | 2.70 | 5.85 | 0.45 |
| 1.3 | 21.49 | 6.73 | 3.15 | 0.28 |
| $step(0.9, 1.1)$ | 21.72 | 5.38 | 4.03 | 0.23 |

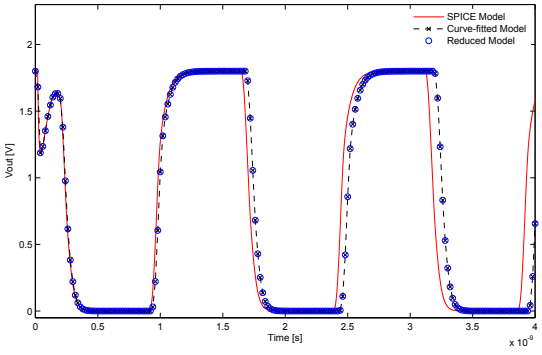


**Figure 7: VCO Output Signal**

## 4.3 Frequency Divider

We consider a Frequency Divider (FD) which is a highly nonlinear circuit commonly used for both analog and digital applications. It inputs a signal of a frequency $f_{in}$ and outputs a signal of frequency $f_{out}$, where $f_{out} = \frac{f_{in}}{n}$ and $n$ is an integer. A typical FD operating frequency ranges from $100MHz$ to $5GHz$. We applied our methodology to reduce

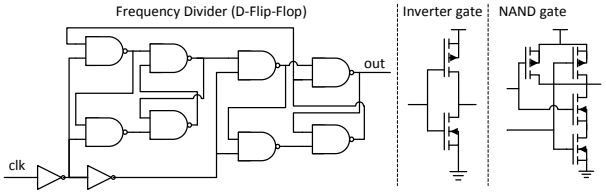


**Figure 8: Frequency Divider Circuit**

the FD implemented using one D-Flip-Flop (eight NAND gates and two inverters), as detailed in Figure 8. This FD is sensitive to the high flank of the input clock signal and output a rectangle signal whose frequency is half of the input clock frequency. The size of the original and reduced FD models are given in Table 5.

**Table 5: Original and Reduced FD Sizes**

| | | | | | |
|---|---|---|---|---|---|
| Original | $C_{cut}^{-1}$ | $G_{cut}$ | $[V;e]$ | $A_I$ | $I(e)$ |
| | $53 \times 53$ | $53 \times 55$ | $55 \times 1$ | $53 \times 36$ | $36 \times 1$ |
| Reduced | $R_l$ | $A_l$ | $z$ | $B_l$ | $u$ |
| | $48 \times 1$ | $48 \times 48$ | $48 \times 1$ | $28 \times 2$ | $2 \times 1$ |

Table 6 summarizes the different simulations performed with the generated reduced FD models for a set of clock frequencies ranging from $0.5GHz$ to $2GHz$. The FD reduced model runs three times faster than the FD original model for a reduction of the state variable size from 53 to 48. The simulation speedup can be increased to higher values by reducing further the state space size and using a sufficient number of linearization points to reproduce the FD behavior at the clock rising and falling edges. Figure 9 shows a snapshot

**Table 6: FD Simulation Results**

| Frequency $[GHz]$ | Run Time$[s]$ | | Speedup | Error $[10^{-2}]$ |
|---|---|---|---|---|
| | Original | Reduced | | |
| 2.0 | 46.80 | 14.56 | 3.21 | 0.18 |
| 1.0 | 43.26 | 15.08 | 2.87 | 0.73 |
| 0.5 | 24.52 | 7.49 | 2.90 | 0.06 |

of FD simulation results reported in row 3 of Table 6. The input clock has a frequency of $2GHz$ and the FD model output has a frequency of $1GHz$. The reduced FD model is as sensitive to the clock edge as the curve-fitted and SPICE models and its output signal accurately reproduces the main frequency component of the SPICE simulation traces.

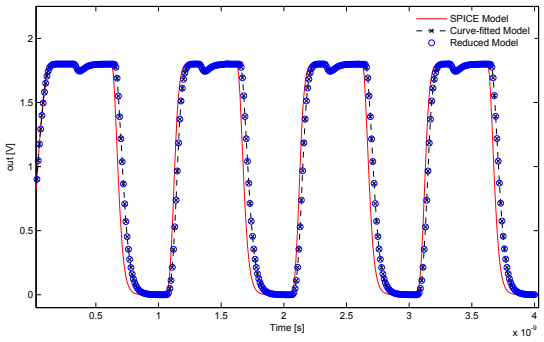


**Figure 9: Frequency Divider Output Signal**

## 5. CONCLUSION

In this paper, we proposed an approach to extract reduced analog circuit models using their SPICE simulation traces. The main challenges of the method are the creation of simplified circuit models via a curve-fitting procedure and their reduction using a Krylov space projection method. Guess functions required by the Levenberg-Marquardt curve-fitting algorithm were obtained with the help of MNA and the use of parametric equivalent models for the active devices. The accuracy of the curve-fitted models was measured by comparing them with the original simulation traces. For that reason, these models are intended to be used for the same input and environment conditions as during the initial SPICE simulation. Otherwise, accuracy issues might raise. The curve-fitted differential models of the circuit are linearized at different points of the state space and are reduced locally via Krylov space projections. The application of the method on three different circuits showed that our reduced models are accurate compared to the simulation traces and are faster than their original models. However, to improve the presented method, curve-fitting could be applied in a hierarchical way after subdividing the original circuit model into sub-circuits with a limited number of active devices. This will reduce the MOR effort and make the method scalable to much larger and complex circuit models. Also, limiting the number of linearization points in each integration time step and using computationally inexpensive weight-functions, which can smooth the model between local regions, can lead to better accuracy and speedup. Finally, to fully automate our methodology, an algorithm has to be implemented for the prediction of the total required linearization points as well as the size of the reduced model based on the information within the simulation traces and the number of nonlinear devices in the circuit netlist.

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