

# A Semi-Formal Approach for Analog Circuits Behavioral Properties Verification

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## ABSTRACT

We propose an environment for the verification of analog circuits behavioral properties, where the circuit state space bounds are first computed using qualitative simulation. Then, their specified behavioral properties are verified on these bounds. The effectiveness of the method is illustrated with a tunnel diode oscillator.

## Categories and Subject Descriptors

B.7.2 [Integrated Circuits]: Design Aids—*Simulation, Verification*

## Keywords

Analog Circuits; Global Optimization; Qualitative Simulation; Tunnel Diode Oscillator

## 1. INTRODUCTION

The analog circuit design process is becoming very complex and therefore new verification approaches are very much needed. Simulation [8] is the most used technique to compute the behavior of a circuit model. Statistical methods like Monte Carlo rely on repeating numerical simulations for a random sampling of parameters. They serve better for fine-tuning parameters and generation of test cases from probability distributions [2]. These two verification methods are not exhaustive and cannot guarantee the coverage of all important corner cases. Formal verification on the other hand ensures exhaustiveness and completeness [10]. For example, in [1, 9] the authors applied formal methods to verify start-up and stability conditions for oscillators. In [4], a formal analysis of SPICE simulation traces was utilized to verify oscillation properties of the Tunnel Diode Oscillator (TDO) with temperature variations. Such contributions are noticeable but they require designer expertise and they poorly scale with the circuit size. Qualitative simulation [7], on the other hand, is a semi formal method for fuzzy dynamical system simulation. It is capable of generating over

approximated envelopes of system trajectories when its parameters and initial conditions are specified as fuzzy distributions. In this work, we propose a framework for modeling and verifying analog circuits behavioral properties based on qualitative simulation.

## 2. PROPOSED METHODOLOGY

An overview of the proposed methodology, implemented in MATLAB [5], is shown in Figure 1. The first block is responsible for generating an augmented differential model for analog circuits described in a SPICE Netlist. To this end, we generate device level models through Modified Nodal Analysis [6]. Then, we augment the obtained differential model with the connection matrix derivatives necessary to compute the circuit behavior for a defined continuous set of conditions. In fact, the elements of this matrix express the sensitivity of the solution. An example of the augmented differential model for the TDO in Figure 2 is shown in Equation (1) (cf. Section 3). The second block computes the state variables bounds of the obtained circuit model for a continuum set of their initial conditions, parameters, inputs or any variable that triggers a specific behavior of the circuit. This block is based on global optimization theory [3] and is inspired from the method for qualitative simulation of fuzzy systems proposed in [7]. The augmented differential model is not solved for every possible situation, but it uses the interior point algorithm to optimize the search for the global extremum. In fact, only the minimum and maximum of each state variable are determined for all specified time points. The result is an over-approximated envelope of all possible model trajectories. Finally, the verification block outputs a pass or fail conclusion when verifying the model properties formulated by the user. The property that can be verified includes model sensitivity, start-up delay, state bounds, or oscillation, as given in Equation (2) (see Section 3).

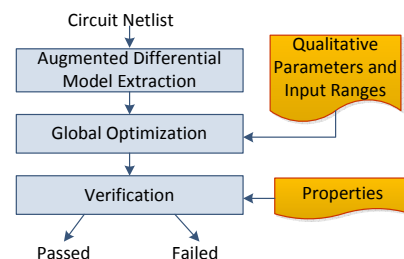


Figure 1: Semi-formal Verification Approach

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### 3. APPLICATION

We consider the TDO shown in Figure 2 and modeled with the augmented differential model given in Equation (1).

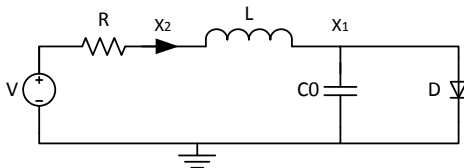


Figure 2: Tunnel Diode Oscillator Schematic

$$\begin{aligned} \dot{x}_1 &= \frac{1}{C0}(-I_d(x_1) + x_2) \\ \dot{x}_2 &= \frac{1}{L}(-x_1 - \frac{1}{G}x_2 + V) \\ \dot{C} &= C \cdot \begin{pmatrix} -\frac{1}{C0}I'_d(x_1) & \frac{1}{C0} \\ -\frac{1}{L} & -\frac{1}{L} \end{pmatrix} \end{aligned} \quad (1)$$

where  $x_1$  is the voltage across the capacitor  $C0 = 1pF$ ,  $x_2$  is the current through the inductor  $L = 1\mu H$ ,  $I_D$  is the current through the diode and  $C$  is a  $2 \times 2$  connection matrix.

We are interested in the effect of the conductance  $G = 1/R$  and the initial conditions  $x_0 \in [[0.4; 0.5]V, [0.4; 0.5]mA]$ , at a nominal temperature ( $T = 200K$ ), on the TDO oscillation property of  $x_1$  and  $x_2$  in  $[0; A_1]$  and  $[0; A_2]$ ,  $A_1 = 0.5V$ ,  $A_2 = 1mA$ , as given in Equation (2).

$$\begin{aligned} (|\text{mean}(x_{imin}) - \frac{A_i}{2}| \leq \varepsilon_1 \wedge |\text{mean}(x_{imax}) - \frac{A_i}{2}| \leq \varepsilon_2) \wedge \\ (|\text{std}(x_{imin}) - \frac{A_i}{2}| \leq \delta_1 \wedge |\text{std}(x_{imax}) - \frac{A_i}{2}| \leq \delta_2), \quad i = 1, 2 \end{aligned} \quad (2)$$

Table 1 reports that the TDO oscillates (Case 1) and locks up (Case 2) and compares our results with the formal method in [4]. In contrast to their method, our approach requires only the differential model and the property expression and covers automatically a complete set of circuit conditions, in reasonable run time and memory usage.

Table 1: TDO Oscillation Property Verification

|                 | Case 1          | Case 2             |
|-----------------|-----------------|--------------------|
| $G$             | $5m\Omega^{-1}$ | $4.13m\Omega^{-1}$ |
| Method in [4]   | Oscillations    | No oscillations    |
| Run time[s]     | 6505.36         | 83835.00           |
| Proposed method | Oscillations    | No oscillations    |
| Run time[s]     | 4076.87         | 3049.95            |
| Mem usage[MB]   | 0.046           | 0.050              |

Figure 3 shows a 2-D state space representation of the oscillation Case 1. By construction, any trajectory originating from the rectangular initial region travels necessarily through the represented rectangular region. Since the complete envelope of the TDO trajectories is oscillating, there is no chance of a lock up scenario in Case 1. Although spurious values which cannot be real solutions of the model are included, the generated boxes are kept tight during the whole simulation time. Figure 4 shows a 2-D state space representation of the lock up Case 2.

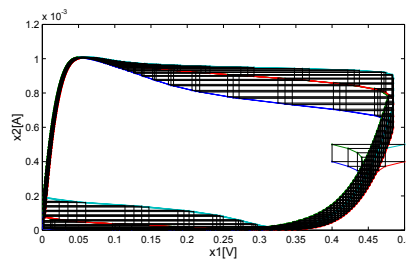


Figure 3: State Space Representation for Case 1

The generated state space regions show that the possible TDO states settle to a fixed region in the state space which eliminates the possibility of a stable oscillation.

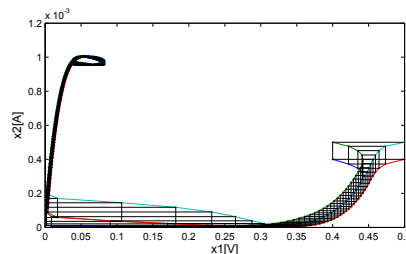


Figure 4: State Space Representation for Case 2

### 4. CONCLUSIONS

We proposed a verification environment to validate behavioral properties of analog circuits based on qualitative simulation. The main advantage of the method is the good coverage of the state space which is sufficient to verify candidate circuit properties in an acceptable run time. The application on the TDO circuit showed that our method is accurate and appealing in terms of efficiency. Future work include the verification of a larger suit of problematic circuits and automating their properties formulation.

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