# Formal Analysis of Power Electronic Systems

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**Abstract.** Power electronics is an active area of research which has widespread applications in safety and cost critical domains such as power grids, biomedical devices and avionics systems. The complexity of power electronic systems is rapidly reaching a point where it will become difficult to verify the correctness and robustness of underlying designs. In this paper, we propose to use a recent formalization of signal-flow-graphs in higher-order-logic for the formal analysis of power electronic converters, which are the foremost components of modern power electronic systems. In particular, we demonstrate the necessary steps to formally reason about the critical properties (e.g., efficiency, stability and resonance) of power electronic converters by using their corresponding signal-flow-graph based high-level models. In order to demonstrate the utilization of the proposed infrastructure, we present the formal analysis of a couple of widely used power converters, namely a pulse width modulation push-pull DC-DC converter and a 1-boost cell DC-DC converter.

## 1 Introduction

Power electronic circuits are networks composed of electronic components and semiconductor devices which are connected together to form a functioning machine or an operational procedure. Nowadays, power electronics is a rapidly expanding field in electrical engineering, where power electronic devices are integral part of our everyday tasks at home, at work and in industrial settings [17]. For example, power electronic converters have found widespread applications in petrochemical [18], water-power stations [17], transportation [3], renewable-energy sources [4] and reactive-power compensators [17]. In the last few decades, high-power devices have been one of the most active areas in research and development of power electronics. Several industrial processes have increased their power needs which are mainly driven by the economy of scale (i.e., production levels and efficiency). In order to cope with future challenges, new paradigms have been developed such as power semiconductors, converter topologies and control methods. As a result, the verification and validation of such systems have become challenging due to the increased design complexities and shorter time-to-market.

One of the core steps in power electronic systems design process is the physical modeling of the circuit components. A significant portion of time is spent


M. Butler et al. (Eds.): ICFEM 2015, LNCS 9407, pp. 270–286, 2015.
DOI: 10.1007/978-3-319-25423-4_17

finding bugs through the validation of such models in order to minimize the failure risks and monetary loss. In particular, this step is more important in the applications, where failures directly lead to monetary loss and safety issues. For example, power electronic convertors are used for pipeline pumps in the petrochemical industry [18] and in grid integration of renewable-energy sources [4]. Generally, there are several kinds of power electronic systems which need to be analyzed; however, the focus of this paper is DC-DC power converts which form the core of power electronic systems. The first step to analyze the behavior of power electronic systems is to obtain the transfer function which relates the input and output signals (voltage or current). Consequently, the test for the stability (which ensures that the system output is always finite) and resonance (which ensures the oscillation of input alternating current at certain frequencies) conditions of the circuit are the foremost design criterion.

Once the stability and resonance of a circuit have been determined, the final step is to obtain the circuit efficiency which is a ratio of output and input powers. One primary analytical approach is to compute the transfer function by explicitly writing node and loop equations which can further be utilized to analyze some physical aspects of power electronic systems. Signal-flow graph (SFG) theory (originally proposed by Mason [13]) has also been used to compute the transfer function of power electronic systems. The main motivation of this choice is inspired by its successful applications to model control systems with minimum mathematical manipulations. Indeed, the problem of finding the transfer function reduces to the identification of forward paths and loops which further can be plugged into the Mason's gain formula (MSG) [14] (which provides an easy way to find the transfer function). Traditionally, the analysis of complex power electronic systems is performed using numerical simulation [24]. To measure the effect of different initial conditions or parametric variation over the circuit operation, it is necessary to perform exhaustive simulations and tests. However, even by doing this, there is no guarantee about the correctness of results, because it is impossible to simulate the system for an infinite number of operating conditions. Another issue of such analysis methods is the approximations in terms of numerical accuracy and types (e.g., real or complex) of variables used to encode the algorithms. For example, a MATLAB program [7] for computing transfer functions treats system parameters as a string of characters; which is indeed a complex-valued function. Considering the above mentioned verification and analysis constraints, we believe that there is a dire need to build a framework which can assist in designing accurate and high assurance power electronic systems.

In recent years, formal methods based techniques (in particular model checking and theorem proving) have been proven to be an effective approach to analyze physical, hybrid and digital engineering systems (e.g., [12]). Despite the fact that formal methods based techniques have the potential to analyze various aspects of physical systems, it is rare to find the usage of formal methods to analyze power electronic systems. The most relevant work for analyzing and modelling power electronic systems using model checking is reported in [15]. However,

the authors do not study the stability and resonance which are critical requirements in designing power electronic systems. Therefore, the main motivation of our work is to fill this gap by proposing a generic framework to analyze power converters. In particular, we review the main functions of our higher-order logic formalization of signal-flow-graph theory along and the Mason's gain formula [2]. We also formalize the notion of stability and resonance along with the formal verification of some important properties such as the finiteness and the cardinality of the set of poles (complex-valued parameters at which the system becomes unstable) and zeros (parameters which determine the resonance condition in the system). In order to demonstrate the practical utilization of our work, we formally verify the transfer functions of 1-boost cell DC-DC converter [24] and push-pull pulse-width-modulation (PWM) DC-DC converter [9]. Consequently, we derive the general stability and resonance conditions, which greatly simplifies the verification for any given circuit configuration. Next, we verify the efficiency of 1-boost cell DC-DC converter circuit. In our work, we use the HOL Light theorem prover [8] due to its rich multivariate analysis libraries and interesting related formalizations about Laplace transform [21] and Z-transform [20]. The source code of our formalization is available for download [1] and can be utilized by other researchers and engineers for further developments and the analysis of various types of power engineering systems.

The rest of the paper is organized as follows: some fundamentals of signal-flow-graph theory and the Mason's gain formula are described in Sect. 2. In Sect. 3, we highlight some definitions of our formalization of signal-flow-graph theory and Mason's gain formula along with the system properties. We present the analysis of the 1-boost cell DC-DC and push-pull PWM DC-DC converters in Sect. 4. Finally, we conclude the paper in Sect. 5.

## 2 Signal-Flow-Graph Theory and Mason's Gain Formula

A signal-flow-graph (SFG) [13] is a special kind of directed graph which is widely used to model engineering systems. Mathematically, it represents a set of linear algebraic equations of the corresponding system. An SFG is a network in which nodes are connected by directed branches. Every node in the network represents a system variable and each branch represents the signal transmission from one node to the other under the assumption that signals flow only in one direction. An example of an SFG is shown in Fig. 2 consisting of five nodes. An input or *source node* and an output or *sink node* are the ones which only have outgoing branches and incoming branches, respectively (e.g., nodes 1 and 5 in Fig. 2). A branch is a directed line from node $i$ to $j$ and the gain of each branch is called the *transmittance*. A *path* is a traversal of connected branches from one node to the other and if no node is crossed more than once and connects the input to the output, then the path is called *forward path*, otherwise if it leads back to itself without crossing any node more than once, it is considered as a *closed path* or a *loop*. A loop containing only one node is called *self loop* and any two loops in the SFG are said to be *touching loops* if they have any common node.

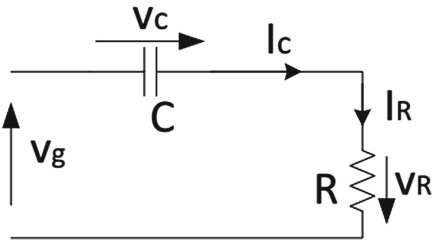


**Fig. 1.** RC circuit

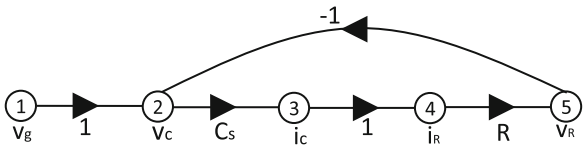


**Fig. 2.** Signal-flow-graph of RC circuit

The total gain of forward path and a loop can be computed by multiplying the transmittances of each traversed branch.

The procedure for transforming power electronic circuits into a signal-flow-graph is straightforward. We start by representing each variable of the circuit as a node in the graph. Next, these nodes are interconnected depending upon their physical behavior in a specific system configuration. The technique of driving-point impedance (DPI) [19] is used to derive the transmittance of the graph branches (capacitor or resistor). Indeed, the DPI analysis is based on the transformation of circuit nodes to their Norton's or Thevenin's equivalent representation along with the application of the principal of superposition [6]. Moreover, Kirchhoff's voltage and current laws are used to derive the relations between voltage and current. Kirchhoff's current law or principle of conservation of electric charge states that at any node (junction) in an electrical circuit, the sum of the currents flowing into that node is equal to the sum of currents flowing out of that node. Kirchhoff's voltage law or the principle of conservation of energy implies that the directed sum of the potential differences around any closed network is zero. For example, consider a simple RC circuit as shown in Fig. 1, where $v_g$ is the input voltage, $v_c$ is the voltage across the capacitor, $i_c$ is the capacitor current, $i_R$ is the resistor current, and $v_R$ is the output voltage. We can transform this circuit into its equivalent signal-flow-graph by finding the set of equations from the physical network of the circuit by first using: Kirchhoff's voltage and current laws for Eqs. 1 and 3, then the branch equations for the capacitor and resistor for Eqs. 2 and 4. The next step consists in assigning to each equation a signal (voltage or current) that will be represented as a node representing each variable of the circuit as a node in the graph. Next, these nodes are interconnected depending upon their physical behavior in a specific system configuration. Note that for each signal-flow-graph a set of independent

equations must be chosen, an equation must only be used once, and the variables of interest must be represented.

$$v_c = v_g - v_R \tag{1}$$
$$i_c = Csv_c \tag{2}$$
$$i_R = i_c \tag{3}$$
$$v_R = Ri_R \tag{4}$$

where $C$ is the capacitance, $R$ is the resistance, and $s$ is the Laplace Transform variable (i.e., $s = \sigma + jw$). Finally, above mentioned results are used to connect the nodes in Fig. 1, to produce the final SFG (Fig. 2). Note that the path from node $v_g$ to node $v_R$ is a forward path whereas the path originating from node $v_c$, traversing $i_c$, $i_R$, $v_R$ and terminating at node $v_c$ forms a loop.

In the analysis of practical engineering systems, the main task is to characterize the relation among system input and output which is called transfer function. The total transmittance or gain between two given nodes (usually input and output) describes the transfer function of the corresponding system. In 1953, Mason [13] proposed a computational procedure (also called Mason's gain formula) to obtain the total gain of any arbitrary signal-flow-graph. The formula is described as follows [14]:

$$G = \sum_k \frac{G_k \Delta_k}{\Delta} \tag{5}$$

$$\Delta = 1 - \sum_m P_{m1} + \sum_m P_{m2} - \sum_m P_{m3} + \ldots + (-1)^n \sum \ldots \tag{6}$$

where $\Delta$ represents the determinant of the graph, $\Delta_k$ represents the value of $\Delta$ for the part of the graph that is not touching the $k^{th}$ forward path and it is called the cofactor of forward path $k$, $P_{mr}$ is the gain product of $m^{th}$ possible combination of $r$ non-touching loops. The gain of each forward path is represented by $G_k$.

For example, we can find the input to output transfer function for the SFG of Fig. 2 using the MGF as follows:

$$\frac{v_R}{v_g} = \frac{RCs}{1 + RCs} \tag{7}$$

## 3 Formalization of Signal-Flow-Graph and Mason's Gain

We model a single branch as a triplet $(a, t_{ab}, b)$, where $a$, $t_{ab}$ and $b$ represent the start node, the transmittance and the end node, respectively. Consequently, a path can be modeled as a list of branches and furthermore an SFG can be defined as a composition of a path along with the information about the total number of nodes in the circuit and the source and the sink nodes at which we

want to compute the transfer function. As mentioned before, nodes and transmittance represent the system variables and gain, respectively. These parameters are indeed complex valued, i.e., $a, t_{ab}, c \in \mathbb{C}$ in the context of power electronic systems. However, the information about the nodes is just used to find properties of signals (current) transmission and they do not appear in the gain and transfer function computation using Mason's gain formula. So, we adapted the same approach as proposed by Mason [13], where nodes of an SFG are represented by natural numbers ($\mathbb{N}$). In order to simplify the reasoning process, we encode the above information by defining three type abbreviations in HOL Light[1], i.e., branch, path and signal-flow-graph as follows:

**Definition 1 (Branch, Path and SFG).**

```
new_type_abbrev ("branch", ‘:ℕ × ℂ × ℕ‘)
new_type_abbrev ("path", ‘:(branch)list‘)
new_type_abbrev ("sfg", ‘:path × ℕ × ℕ × ℕ‘)
```

where the second, third, and the fourth elements of `sfg` represent the size, the output node and the input node of a signal-flow-graph, respectively.

Our next main task is to find all the forward paths and loops from the source node to the sink node given by the user. We implemented a search algorithm proposed in [23] which considers each path only once during the search.

In our formalization, we add a skipping function which helps to ignore the nodes which do not have any incoming branches. Indeed, we cannot find a loop which contains a node that does not have incoming branches from the definition of a feedback loop. Hence, the skipping function greatly improves the performance of the search algorithm. Briefly, in our formalization, we take an SFG and generate a matrix in which nodes are arranged in the first column and each row represents the branches of the node under consideration. For feedback loops extraction, we start the process by the first node of the SFG and we go through all possible paths which start from the node under consideration and test for each path whether it is a loop or not. In the next iteration, we go to the next node of the graph and repeat the same process. For forward paths extraction, we repeat a similar process, but we only consider the paths starting from the source node rather than exploring all the nodes.

For the sake of conciseness, we present a list of some of the main functions of our formalization of signal-flow-graph theory with a brief description in Table 1, while more details can be found in [2].

Finally, we utilize the definitions described in Table 1 to formalize the Mason's gain formula given in Eq. 5, as follows:

**Definition 2 (Mason's gain formula).**

```
⊢ ∀(system : sfg). Mason_Gain system =
    PRODUCT_FORWARD_DELTA (EC system) (FC system)
    ---------------------------------------------
              DETERMINANT (EC system)
```

[1] In this paper, we use minimal HOL Light syntax in the presentation of definitions and theorems to improve the readability.

**Table 1.** Some important functions of SFG formalization

| Definition | Description | Formalization |
|---|---|---|
| ECSKIP | Skip the process of finding loops of nodes that do not have incoming branches | ⊢ ∀ (p:ℕ) (G:(ℕ list) list) (n:ℕ) (m:ℕ). ECSKIP p G m n = if($m = n$) then F else if(p ∈ $G[m]$) then T else (ECSKIP p G (m+1) n) |
| EC_POINT | Extract all the feedback loops which start from a given point of the graph | ⊢ ∀ (l:KPH) (G:(ℕ list) list) (t:ℕ list). EC_POINT l G [ ] = [ ] ∧ EC_POINT l G (CONS e t) = if((fst_of_trpl l = 0) ∧ (¬(EC_TEST (snd_of_trpl l) (fst_of_trpl l) G))) then [ ] else (APPEND (if(EC_TEST (snd_of_trpl l)(fst_of_trpl l) G) then [(EC_add_node (snd_of_trpl l))] else [ ]) (EC_POINT (EC_POINT_AID l G) G t3)) |
| FC | Extract all the forward paths in a given SFG | ⊢ ∀ (l:path) (size:ℕ) (stop:ℕ) (start:ℕ). FC l size stop start = if(l = [ ]) then [ ] else FC_REWRITING (FC_MAIN l size stop start) l |
| IS_TOUCHING | Check if two paths have common nodes | ⊢ ∀ (t1:path) (t2:path). IS_TOUCHING [ ] [ ] = F ∧ IS_TOUCHING t2 [ ] = F ∧ IS_TOUCHING [ ] t1 = F ∧ IS_TOUCHING (CONS a t1) (CONS b t2) = if ((RIGHT (CONS a t1) b) ∨ (LEFT a (CONS b t2))) then T else IS_TOUCHING t1 t2 |
| DETERMINANT | Compute the determinant of the given graph | ⊢ ∀ (t:(path) list). DETERMINANT t = 1 + (DELTA_MINUS_ONE t (TOUCHING_LOOP_MAIN t) t (TOUCHING_LOOP_MAIN t)) |
| PRODUCT_FORWARD_DELTA | Compute the numerator of the graph according to Mason's gain formula | ⊢ ∀ (t1:(path)list) (t2:(path)list). PRODUCT_FORWARD_DELTA [ ] t2 = Cx(&0) ∧ PRODUCT_FORWARD_DELTA (CONS f t1) t2 = ((GAIN f) * (1 + FORWARD_DELTA_MINUS f t2 + PRODUCT_FORWARD_DELTA t1 t2) |

where the function `Mason_Gain` accepts an SFG (i.e., `system`, which is a model of the given system in our case) and computes the Mason's gain as given in Eq. 5. Note that the function `PRODUCT_FORWARD_DELTA` accepts the list of loops (computed by `EC`) and forward paths (computed by `FC`) in the system and computes $\sum_{k \in system} G_k \Delta_k$, where $G_k$ and $\Delta_k$ represent, respectively, the product of all forward path gains and the determinant of the $k^{th}$ forward path considering the elimination of all loops touching the $k^{th}$ forward path as described in Sect. 2. The function `DETERMINANT` takes the list of loops and gives the determinant of the system as described in Eq. (6).

In practice, the physical behavior of any power electronic system is described by the transmittance of each path (or a single branch) involved in the signal-flow-graph. We can consider each path as a system component which processes the input current signal to achieve the desired functionality. Indeed, the SFG of the given power electronic system is expressed as a function of the parameter "$s$" and we need to consider this physical aspect in the formalization of the transfer function which describe the overall behavior of the system. It is mentioned in Sect. 2 that the Mason's gain formula describes the total gain between the input and the output of the system and hence it can be used to describe the transfer function of the power electronic system provided the given signal-flow-graph can be described as a function of a complex parameter "$s$". We use the Mason's gain formalization and the above description to formalize the transfer function of a given power electronic system as follows:

**Definition 3 (System Transfer Function).**

$\vdash \forall$ `system. transfer_function system = Mason_Gain (λs. system s)`

where the function `transfer_function` accepts a `system` which has type $\mathbb{C} \rightarrow$ `sfg` and returns a complex ($\mathbb{C}$) number which represents the transfer function of the power electronic system (i.e., `system`).

We have automatized the different steps for finding the transfer function of any arbitrary signal-flow-graph by developing some new simplification tactics using derived rules and tactics of HOL Light. In terms of automation, these tactics can be divided into three varieties: the first proves the extracted list of feedbacks, the second proves the extracted list of forward paths, and the third proves Mason's gain formula. In Table 2, we provide some of these tactics with corresponding descriptions. Using these tactics we prove all transfer functions given in [1]. The availability of these tactics provides the effective automation to the user, so that an application to a particular system does not involve the painful manual proofs often required with interactive theorem proving. Developing such tactics represents a first step towards building an automated tool to carry the verification of transfer functions of power electronic circuits on the basis of their signal-flow-graphs representations.

**Table 2.** HOL automation tactics

| Tactic | Description |
|---|---|
| `TAC_FC` | Simplify the function which computes the entire list of forward paths. |
| `TAC_EC` | Simplify the function which computes the entire list of feedback paths. |
| `MASON_SIMP_TAC` | Simplify the function which computes the transfer function using MGF. |
| `COMPLEX_DIV_TAC` | Simplify a goal which is expressed as a fractional expression. |
| `SFG_TAC` | Main tactic for simplifying the transfer function of a given SFG. |

### 3.1 Formalization of System Properties

In order to verify that the given model meets its specification, we need to build the foundations based on which we can formally describe the main system properties (i.e., stability, resonance) in HOL. Physically, the stability and resonance are concerned with the identification of all the values of $s$ for which the system transfer function becomes infinite and zero, respectively. In the control theory literature, these values are called *system poles* and *system zeros* which can be computed by the denominator and numerator of the transfer function, respectively. Furthermore, all poles and zeros need to be inside the unit circle which means that their magnitude should be less or equal to 1. We formalize the above mentioned informal description of the system properties in HOL as follows:

**Definition 4 (System Poles).**

$$\vdash \forall\ \texttt{system.}\ \texttt{poles system} = \{\texttt{s} \mid \texttt{denominator (system s)} = 0\}$$
$$\vdash \forall\ \texttt{system.}\ \texttt{zeros system} = \{\texttt{s} \mid \texttt{numerator (system s)} = 0\}$$

where the functions `poles` and `zeros` take the `system` as a parameter and return the set of poles and zeros, respectively. Next, we formalize the notion of stability and resonance as follows:

**Definition 5 (System Stability and Resonance).**

$$\vdash \forall\ \texttt{system. is\_stable system}\ [\texttt{p}_0, ..., \texttt{p}_\texttt{n}] \Leftrightarrow$$
$$\forall \texttt{p}_\texttt{i}.\ \texttt{p}_\texttt{i} \in (\texttt{poles system}) \wedge \parallel \texttt{p}_\texttt{i} \parallel \leq 1$$
$$\vdash \forall\ \texttt{system. is\_resonant system}\ [\texttt{z}_0, ..., \texttt{z}_\texttt{n}] \Leftrightarrow$$
$$\forall \texttt{z}_\texttt{i}.\ \texttt{z}_\texttt{i} \in (\texttt{zeros system}) \wedge \parallel \texttt{z}_\texttt{i} \parallel \leq 1$$

where the predicate `is_stable` accepts the power electronic system signal-flow-graph model (i.e., `system`) and a list of poles $[\texttt{p}_0, ..., \texttt{p}_\texttt{n}]$ and verifies that each element $p_i$ is indeed a pole of the system and its corresponding magnitude (i.e., norm of a complex number, $\parallel \texttt{p}_\texttt{i} \parallel$) is smaller or equal to 1. The predicate `is_resonant` is defined in a similar way by considering the list of zeros instead of the list of poles of the system.

Next, we verify an important theorem which describes that if the denominator or the numerator of the transfer function is a polynomial of order $n$, it will always have a finite number of poles or zeros and the cardinality of the set of poles and zeros can only be equal or less than $n$.

**Theorem 1 (Finiteness and Cardinality of poles and zeros).**

$$\vdash \forall \texttt{n c system.}\ \neg(\forall\ \texttt{i.}\ \texttt{i} \in \{0, 1, ..., \texttt{n}\} \Rightarrow \texttt{c i} = 0) \wedge$$
$$(\forall\ \texttt{z.}\ \texttt{denominator (system z)} = \sum_{\texttt{i} \in \{0,1,...,\texttt{n}\}} (\lambda \texttt{i.}\ \texttt{c i} * \texttt{z}^\texttt{i})) \implies$$
$$\texttt{FINITE (poles (system z))} \wedge\ \texttt{CARD (poles (system z))} \leq \texttt{n}$$

where `n` represents the order of the complex polynomial function `c`. The functions `FINITE` and `CARD`, represent the finiteness and cardinality of a set, respectively. We also prove the same theorem for the set of zeros of a system, where more details can be found at [1].

This concludes the signal-flow-graph formalization and system properties. In the next section, we will show how to apply our formalization in practice by presenting the formal analysis of two important topologies of power converters using the previously presented theorems and definitions.

## 4 Application: Power Electronics Systems

Power electronics has found an important place in modern technology being a core of power and energy control. Generally, the interaction between the utility and the load depends on the topology of the power system. Most of electronic supplies are switching semiconductor converters thanks to theirs efficiency. Power electronic converters are constructed by electronic devices, driving, protection and control circuits. In particular, DC-DC converters change the DC voltage and current levels using the switching mode of semiconductor devices. As a rule, they provide means for changing and stabilizing the output DC voltage. A DC-DC converter consists of the switching circuitry and the filter section, and power converters with feedback are known as regulators. Power electronics converters must be suitably controlled to supply the voltages, currents, or frequency ranges needed for the load and to guarantee the requested power quality. In the following subsections, we present the formal analyses of two topologies of power electronic circuits in higher-order-logic using the previous formalization.

### 4.1 1-Boost Cell Interleaved DC-DC Converter

Interleaved DC-DC converters are composed of N-boost cells connected in parallel which operate in an interleaved fashion. The elementary cell can be a two-level or multi-level DC-DC converter. The elementary DC-DC cells are driven with pulse width modulation in which pulses are shifted by $\frac{2\pi}{N}$ radians. Some of the advantages of interleaved parallel converters are the ripple cancellation both in the input and output waveforms and lower value of ripple amplitude. Interleaved DC-DC converter are widely used in various critical power conversion applications, such as voltage regulation modules [10], and automotive applications. Thus they have been used in aircrafts, to increase flight performance (e.g., thrust and maneuverability) and enhance onboard mission capability (e.g., sensors, weapons and communication) [11].

In [24], the authors proposed to use SFG to model N-boost cells interleaved DC-DC converters and they illustrate the analysis for the case of 1-boost cell, 2-boost cells and 3-boost cells interleaved parallel converters. We use our proposed framework to formally analyze 1-boost cell, 2-boost cells, and 3-boost cells interleaved parallel converters. For the sake of conciseness, we present the analysis of a 1-boost cell interleaved parallel converter only and more details about the 2-boost and 3-boost cells interleaved converters can be found in [1].

The circuit representation of 1-boost cell interleaved parallel DC-DC converter system is shown in Fig. 3. The circuit parameters $L_1$, $D_1$, and $r_1$ represent the inductance of individual boost cell, the duty ratios of the $1^{st}$ state, and the inductor series resistance, respectively. The parameters $R$ and $C$ are the load resistance and the circuit capacitor, respectively. The parameters $V_g$, $I_g$ and $V_1$ are the supply voltage, the source current and the voltage across inductor, respectively. Similarly, $V_0$ and $I_0$ are the output voltage and the output current, respectively. The SFG model of 1-boost cell interleaved parallel DC-DC converter is shown in Fig. 4.

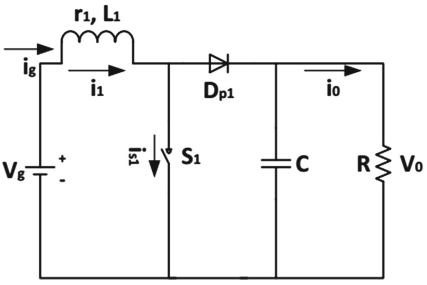


**Fig. 3.** 1-Boost Cell DC-DC Converter

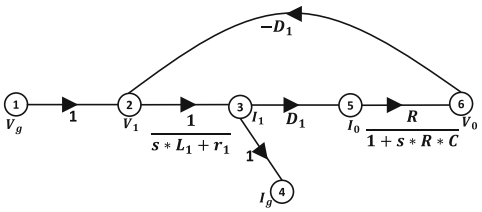


**Fig. 4.** SFG of 1-Boost Cell DC-DC Converter

Our main interest is to evaluate the circuit behavior at the output node which is represented by node ⑥[2], when the signal is applied at the input, i.e., node ①. We keep all above mentioned parameters in the general form which further can be used to model different 1-boost cell DC-DC converter circuit configurations. We formally define 1-boost cell DC-DC converter in HOL as follows:

**Definition 6 (1-Boost Cell DC_DC Converter Model).**

$$\vdash \forall\ \mathtt{C}\ \mathtt{R}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s}\ \in \mathbb{C}.$$
$$\mathtt{DC\_model}\ \mathtt{R}\ \mathtt{C}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s} =$$
$$([(1,1,2);(2,\tfrac{1}{\mathtt{s}*\mathtt{L_1}+\mathtt{r_1}},3);(3,1,4);(3,\mathtt{D_1},5);(5,\tfrac{\mathtt{R}}{1+\mathtt{s}*\mathtt{R}*\mathtt{C}},6);(6,-\mathtt{D_1},2)],6,6,1)$$

where `DC_model` accepts complex-valued circuit parameters, and returns the signal-flow-graph which has 6 nodes, where the output node is ⑥ and the input node is ① as shown in Fig. 4. Next, we verify the transfer function of the 1-boost cell DC-DC converter circuit as follows:

**Theorem 2 (Transfer Function of 1-Boost Cell DC_DC Converter).**

$$\vdash \forall\ \mathtt{C}\ \mathtt{R}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s} \in \mathbb{C}.$$
$$(1+\mathtt{s}*\mathtt{R}*\mathtt{C} \neq 0)\ \wedge\ (\mathtt{s}*\mathtt{L_1}+\mathtt{r_1} \neq 0)\ \Longrightarrow$$
$$\mathtt{transfer\_function}\ (\mathtt{DC\_model}\ \mathtt{R}\ \mathtt{C}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s}) =$$
$$\frac{\mathtt{D_1}*\mathtt{R}}{\mathtt{R}*\mathtt{C}*\mathtt{L_1}*\mathtt{s}^2+(\mathtt{R}*\mathtt{C}*\mathtt{r_1}+\mathtt{L_1})*\mathtt{s}+\mathtt{r_1}+\mathtt{D_1}^2*\mathtt{R}}$$

The proof of this theorem is mainly based on the extraction of forward paths and feedback loops in the circuit and then using the Mason's gain formula. We have

[2] Here the output node has an outgoing branch that does not follow the conventional designation of output (e.g., no outgoing branches). However, the transfer function is the same as the one obtained by adding a new output node and connecting it to the node ⑥ with transmittance equal to 1. Therefore, for the sake of simplicity, we did not add a new node that does not have physical meaning in the circuit.

made efforts to provide the effective automation using derived rules and tactics, so that the application to a particular system does not involve the painful manual proofs often required with interactive (higher-order logic) theorem proving. For example, the formal proof of Theorem 2 requires only three lines of HOL light code. A brief summary of developed tactics can be found in [2] (Appendix I).

The efficiency of any system is the useful power output divided by the total electrical power consumed. As the power in electronic circuit is the product of the voltage ($V$) and current ($I$), we can define the 1-boost cell DC-DC converter efficiency as follows:

**Definition 7 (1-Boost Cell DC_DC Converter Efficiency).**

$$\vdash \forall\ \mathtt{R}\ \mathtt{C}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s}\ \in \mathbb{C}.\quad \mathtt{Efficiency}\ (\mathtt{DC\_model}\ \mathtt{R}\ \mathtt{C}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s}) = \frac{\mathtt{I_0} * \mathtt{V_0}}{\mathtt{I_g} * \mathtt{V_g}} = \frac{\mathtt{V_0}}{\mathtt{V_g}} * \frac{\mathtt{V_g}}{\mathtt{I_g}} * \frac{\mathtt{I_0}}{\mathtt{V_g}}$$

Repeating the same process for calculating the transfer function in Theorem 2 we can compute the transfer functions of $\frac{I_g}{V_g}$ and $\frac{I_0}{V_g}$ by replacing the output node ⑤ by ④ and ⑥, respectively.

Based on the three transfer functions and the Definition 7 of the efficiency, we can prove the expression of the efficiency of 1-boost cell converter as follows:

**Theorem 3 (1-Boost Cell DC_DC Converter Efficiency).**

$$\vdash \forall\ \mathtt{C}\ \mathtt{R}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s}\ \in \mathbb{C}.\quad (1 + \mathtt{s} * \mathtt{R} * \mathtt{C} \neq 0) \wedge (\mathtt{s} * \mathtt{L_1} + \mathtt{r_1} \neq 0) \wedge (\mathtt{R} * \mathtt{C} * \mathtt{L_1} * \mathtt{s}^2 + (\mathtt{R} * \mathtt{C} * \mathtt{r_1} + \mathtt{L_1}) * \mathtt{s} + \mathtt{r_1} + \mathtt{D_1}^2 * \mathtt{R} \neq 0) \Longrightarrow \mathtt{Efficiency}\ (\mathtt{DC\_model}\ \mathtt{R}\ \mathtt{C}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s}) = \frac{\mathtt{D_1}^2 * \mathtt{R}}{\mathtt{R} * \mathtt{C} * \mathtt{L_1} * \mathtt{s}^2 + (\mathtt{R} * \mathtt{C} * \mathtt{r_1} + \mathtt{L_1}) * \mathtt{s} + \mathtt{r_1} + \mathtt{D_1}^2 * \mathtt{R}}$$

The denominator of the transfer function of 1-boost cell DC-DC converter can be represented as a second order polynomial which leads to the useful information that the 1-boost cell DC-DC circuit can only have 2 poles at maximum according to Theorem 1. Next, we present the verification of the stability conditions of the 1-boost cell DC-DC convertor circuit as follows:

**Theorem 4 (Stability Conditions for 1-Boost Cell DC_DC Converter).**

$$\vdash \forall \mathtt{G_1}\ \mathtt{G_2}\ \mathtt{G_3}\ \mathtt{k_1}\ \mathtt{k_2}\ \in \mathbb{C}.\quad \left\| \frac{-(\mathtt{R}*\mathtt{C}*\mathtt{r_1}+\mathtt{L_1}) \pm \sqrt{(\mathtt{R}*\mathtt{C}*\mathtt{r_1}+\mathtt{L_1})^2 - 4*\mathtt{R}*\mathtt{C}*\mathtt{L_1}*(\mathtt{r_1}+\mathtt{D_1^2}*\mathtt{R})}}{2*\mathtt{R}*\mathtt{C}*\mathtt{L_1}} \right\| \leq 1 \wedge \frac{(\mathtt{R}*\mathtt{C}*\mathtt{r_1}-\mathtt{L_1}) \pm \sqrt{(\mathtt{R}*\mathtt{C}*\mathtt{r_1}+\mathtt{L_1})^2 - 4*\mathtt{R}*\mathtt{C}*\mathtt{L_1}*(\mathtt{r_1}+\mathtt{D_1^2}*\mathtt{R})}}{2*\mathtt{R}*\mathtt{C}*\mathtt{L_1}} \neq 0 \wedge \frac{(\mathtt{L_1}-\mathtt{R}*\mathtt{C}*\mathtt{r_1}) \pm \sqrt{(\mathtt{R}*\mathtt{C}*\mathtt{r_1}+\mathtt{L_1})^2 - 4*\mathtt{R}*\mathtt{C}*\mathtt{L_1}*(\mathtt{r_1}+\mathtt{D_1^2}*\mathtt{R})}}{2*\mathtt{R}*\mathtt{C}*\mathtt{L_1}} \neq 0 \wedge \Longrightarrow \mathtt{is\_stable}\ (\lambda \mathtt{s}.\ (\mathtt{DC\_model}\ \mathtt{R}\ \mathtt{C}\ \mathtt{D_1}\ \mathtt{r_1}\ \mathtt{L_1}\ \mathtt{s})$$

$$\left[\frac{-(\mathtt{R}*\mathtt{C}*\mathtt{r}_1+\mathtt{L}_1)-\sqrt{(\mathtt{R}*\mathtt{C}*\mathtt{r}_1+\mathtt{L}_1)^2-4*\mathtt{R}*\mathtt{C}*\mathtt{L}_1*(\mathtt{r}_1+\mathtt{D}_1^2*\mathtt{R})}}{2*\mathtt{R}*\mathtt{C}*\mathtt{L}_1};\right.$$
$$\left.\frac{-(\mathtt{R}*\mathtt{C}*\mathtt{r}_1+\mathtt{L}_1)+\sqrt{(\mathtt{R}*\mathtt{C}*\mathtt{r}_1+\mathtt{L}_1)^2-4*\mathtt{R}*\mathtt{C}*\mathtt{L}_1*(\mathtt{r}_1+\mathtt{D}_1^2*\mathtt{R})}}{2*\mathtt{R}*\mathtt{C}*\mathtt{L}_1}\right]$$

where $\| \, . \, \|$ and $\sqrt{.}$ represent the complex norm and complex square root, respectively. The first assumption is required to prove that both poles are inside the unit circle, and the following two assumptions ensure that poles are not equal to $-\frac{r_1}{L_1}$, $-\frac{1}{R*C}$, respectively.

This concludes our HOL formal analysis of the 1-boost cell DC-DC converter circuit. The source code of the circuit formalization and the analysis of the 2-boost and 3-boost cells DC-DC converters circuits can be found in [1].

### 4.2 Pulse Width Modulation Push-Pull DC-DC Converter

Pulse width modulated (PWM) push-pull DC-DC converters are very popular in modern power electronic supplies. They have many applications in some sensitive and critical areas such as aerospace, transportation, and renewable energy [4]. Hence, a robust and secure stability analysis of this type of converter is extremely important. A PWM constant-frequency control technique is considered as one of the most widely used component in switched-mode DC-DC power supplies. Voltage-mode and current-mode controllers allow for achieving a satisfactory dynamic performance of DC-DC converters is considered as a DC-DC converter operating under switched-load conditions.

The circuit of linearized model of the power stage with a variable load current of PWM push-pull converter is shown in Fig. 5. In the circuit, $v_c$ is the voltage across the capacitor C, $v_T$ is the averaged control voltage (input voltage), $i_o$ is the converter output current, $v_o$ is the converter output voltage, $L$ is the indicator, $r$ is the equivalent averaged resistance in series with the inductor, and $r_c$ is the equivalent series resistance of the capacitor.

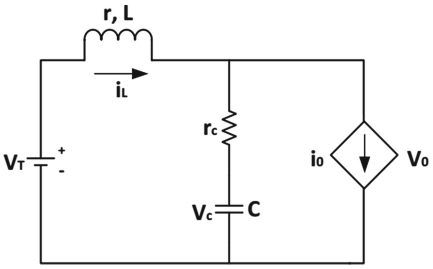


**Fig. 5.** Linearized model of PWM Push Pull DC-DC Converter

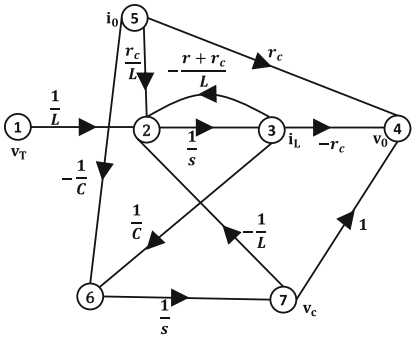


**Fig. 6.** SFG of PWM Push Pull DC-DC Converter

In [9], the authors proposed a block diagram of closed-loop of the circuit (circuit with the gains of compensation and feedback loop from the output to the input). The block diagram equivalent signal-flow-graph of PWM push-pull converter without the control part is shown in Fig. 6. The SFG is composed of 7 nodes the input node is 1 ($V_T$ in [9]) and the output node is 4 ($V_o$ in [9]).

**Definition 8 (PWM Push Pull DC-DC Converter Model).**

$$\begin{aligned}&\vdash\ \forall\ \mathtt{C}\ \mathtt{L}\ \mathtt{r}\ \mathtt{k_y}\ \mathtt{r_c}\ \mathtt{k_i}\ \mathtt{k_v}\ \mathtt{s}\ \in \mathbb{C}.\\ &\quad \mathtt{PWM\_model}\ \mathtt{C}\ \mathtt{L}\ \mathtt{r}\ \mathtt{k_y}\ \mathtt{r_c}\ \mathtt{k_i}\ \mathtt{k_v}\ \mathtt{s}\ =\\ &([(1,\tfrac{1}{\mathtt{L}},2);(2,\tfrac{1}{\mathtt{s}},3);(3,\tfrac{-(\mathtt{r}+\mathtt{r_c})}{\mathtt{L}},2);(3,-\mathtt{r_c},4);(3,\tfrac{1}{\mathtt{C}},6);(5,\mathtt{r_c},4);\\ &(5,-\tfrac{1}{\mathtt{C}},6);(5,\tfrac{\mathtt{r_c}}{\mathtt{L}},2);(6,\tfrac{1}{\mathtt{s}},7);(7,-\tfrac{1}{\mathtt{L}},2);(7,1,4)],7,4,1)\end{aligned}$$

where `PWM_model` accepts complex-valued circuit parameters, and returns the signal-flow-graph which has a total number of 7 nodes where the output node is ④ and the input node is ① as shown in Fig. 6.

Next, we verify the transfer function of the PWM push-pull DC-DC converter circuit as follows:

**Theorem 5 (Transfer Function of PWM).**

$$\begin{aligned}&\vdash\ \forall\ \mathtt{C}\ \mathtt{L}\ \mathtt{r}\ \mathtt{r_c}\ \mathtt{s}\ \in \mathbb{C}.\\ &\quad (\mathtt{L}*\mathtt{C}\neq 0)\ \Longrightarrow\\ &\ \mathtt{transfer\_function}\ \mathtt{PWM\_model}\ \mathtt{C}\ \mathtt{L}\ \mathtt{r}\ \mathtt{r_c}\ \mathtt{s}\ =\\ &\qquad \frac{1-\mathtt{s}*\mathtt{C}*\mathtt{r_c}}{\mathtt{C}*\mathtt{L}*\mathtt{s}^2+(\mathtt{r_c}+\mathtt{r})*\mathtt{C}*+1}\end{aligned}$$

Next, we present the verification of the stability conditions of the PWM push-pull DC-DC converter circuit under the circuit global parameters as follows:

**Theorem 6 (Stability Conditions for PWM).**

$$\begin{aligned}&\vdash\ \forall\ \mathtt{C}\ \mathtt{L}\ \mathtt{r}\ \mathtt{r_c}\ \in \mathbb{C}.\\ &\quad \| \tfrac{-(\mathtt{r}+\mathtt{r_c})*\mathtt{C}\mp\sqrt{((\mathtt{r}+\mathtt{r_c})*\mathtt{C})^2-4*\mathtt{C}*\mathtt{L}}}{2*\mathtt{C}*\mathtt{L}} \|\leq 1\ \wedge\\ &\quad \tfrac{-(\mathtt{r}+\mathtt{r_c})*\mathtt{C}\pm\sqrt{((\mathtt{r}+\mathtt{r_c})*\mathtt{C})^2-4*\mathtt{C}*\mathtt{L}}}{2*\mathtt{C}*\mathtt{L}} \neq 0\ \wedge \mathtt{L}*\mathtt{C}\neq 0\ \Longrightarrow\\ &\quad \mathtt{is\_stable}\ \ (\lambda \mathtt{s}.\ \mathtt{PWM\_model}\ \mathtt{C}\ \mathtt{L}\ \mathtt{r}\ \mathtt{r_c}\ \mathtt{s}\ )\ \mathtt{s}\\ &\quad [\tfrac{-(\mathtt{r}+\mathtt{r_c})*\mathtt{C}+\sqrt{((\mathtt{r}+\mathtt{r_c})*\mathtt{C})^2-4*\mathtt{C}*\mathtt{L}}}{2*\mathtt{C}*\mathtt{L}};\ \tfrac{-(\mathtt{r}+\mathtt{r_c})*\mathtt{C}-\sqrt{((\mathtt{r}+\mathtt{r_c})*\mathtt{C})^2-4*\mathtt{C}*\mathtt{L}}}{2*\mathtt{C}*\mathtt{L}}]\end{aligned}$$

The first assumption ensures that both poles are inside the unit circle, whereas the second assumption is required to prove that the poles are not equal to zero. Similarly, we verify the resonance condition for the PWM push-pull DC-DC converter circuit as follows:

**Theorem 7 (Resonant Conditions for PWM).**

$$\begin{aligned}&\vdash\ \forall\ \mathtt{C}\ \mathtt{L}\ \mathtt{r}\ \mathtt{r_c}\ \in \mathbb{C}.\\ &\quad \| \tfrac{1}{\mathtt{C}*\mathtt{r_c}} \|\leq 1\ \wedge\ \mathtt{r_c}\neq 0\ \wedge\ \mathtt{L}*\mathtt{C}\neq 0\ \Longrightarrow\\ &\quad \mathtt{is\_resonant}\ \ (\lambda \mathtt{s}.\ \mathtt{PWM\_model}\ \mathtt{C}\ \mathtt{L}\ \mathtt{r}\ \mathtt{r_c}\ \mathtt{s}\ )\ \mathtt{s}\ [\frac{1}{\mathtt{C}*\mathtt{r_c}}]\end{aligned}$$

The assumptions in theorem ensure that the systems zero is inside the unit circle and it is not equal to zero.

Note that the stability and resonance conditions are verified under the general parameters of the PWM circuit (e.g., $r$, $r_c$, $L$,...) and 1-boost cell circuit (e.g., $L_1$, $D_1$, $r_1$,...) which is not possible in the case of simulation. One of the main strengths of the theorem proving based approach is to unveil all the assumptions under which a theorem can be verified. For example, most of the assumptions in Theorems 4, 6, and 7 are not mentioned in the paper-and-pencil analyses reported in [9,24]. However, without these assumptions these theorems cannot be verified. Moreover, our results are verified under universal quantifiers and the problem of finding the stability and resonance conditions reduces to just ensuring that the values of the system parameters satisfy the assumptions. Remark that the signal-flow-graph models of the two applications involve, respectively, 6 and 8 nodes SFGs, however, our formalization is general and can be applied for an arbitrary number of nodes. For example, in [5] we have formally verified the transfer function of an application which consists of 20 nodes and 14 complex-valued parameters.

We believe that the formal analysis of above mentioned two real-world power electronic systems provides two main indications: theorem proving systems have reached to the maturity, where complex physical models can be expressed with less efforts than ever before; and formal methods can assist in the verification of power electronic systems which are rapidly reaching a point where it will be impossible to verify correctness of the design and its robustness. In reality, verification tools must be largely automatic to be effectively adopted which limits the usage of interactive theorem prover in industry. On the other hand, computer algebra systems (CASs), e.g., Mathematica, are more popular than theorem provers. The most important reason is that CAS tools are easier to use, and are also increasingly applied in education, which is not the case for theorem provers. Another important factor is the rapidity of CAS tools compared to theorem provers. However, higher-order-logic theorem proving systems are more precise and reliable. Our reported work can be considered as a one step towards an ultimate goal of building automatic tools which make use of HOL theorem provers as a certification tool in the design and analysis cycles of safety-critical real-world systems from different engineering and physical science disciplines (e.g., signal processing, control systems, power electronics, biology, optical and mechanical engineering).

## 5 Conclusion

In this paper, we reported a new application of formal methods in the domain of power electronics. We presented a formal analysis framework based on higher-order logic which provides the required expressiveness and soundness to formally model and verify physical aspects of power electronic systems. In particular, we presented an overview of our formalization of the signal-flow-graph theory along with the Mason's gain formula and transfer functions. Similarly, we presented the

formalization of the properties of the power electronic systems. Consequently, we derive the transfer function of two real-world power electronic applications which are 1-boost cell DC-DC converter and PWM push pull DC-DC converter. Finally, we described the formal analysis of the stability and resonance conditions of these two applications.

Our immediate future work is to formally verify a couple of key properties about the forward and feedback paths extraction: (1) each path is extracted only once; (2) the transfer function of transposed SFG [16] is the same as the original one. This requires the formalization of undirected signal-flow-graph [22]. We also plan to verify more complex power electronic engineering systems along with the formal relation among the signal-flow-graph representation and the Z-transform [20] and the Laplace Transform [21]. A potential utilization of our formalization and developed automation tactics is to build a framework to certify the results produced by informal tools such as MATLAB based SFG analysis program (available at [7]).

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