Using Stochastic Differential Equation for Assertion Based Verification of Noise in Analog/RF Circuits

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***Abstract*—Today's analog/RF design and verification face significant challenges due to circuit complexity and short market windows. In particular, the issues related to noise modeling and verification still remains a priority for many applications. In this paper, we propose a methodology for modeling and verification of analog/RF designs in the presence of noise. Our approach is based on modeling the designs using stochastic differential equations (SDE) to incorporate the statistical nature of noise. Then, we define an assertion based verification method integrated in the SDE simulation framework for monitoring properties of interest in order to quickly detect errors. Our approach is illustrated on nonlinear tunnel-diode and Colpitts oscillators circuits.**

I. Introduction

In recent years, advanced technologies has allowed designers to develop smaller, faster, low power integrated analog/RF/digital designs in a single chip, known as systems-on-a-chip (SoCs). Their goal is to address the need for higher performance and functionality in applications such as multimedia, wireless, telecommunications, etc. However, this complex integration among various blocks has brought in additional challenges to the design and verification process due to nonlinear dynamics of analog/RF designs. For instance, in the case of communication and signal processing designs, noise generated from different parts of the circuit elements (passive and active) has a direct impact on the performance of the design [20]. In general, the sources of noise could be due to unwanted interaction between the circuit elements (e.g., cross-talk noise) or it could be inherited from the circuit elements (e.g., thermal, shot and flicker) [21]. However, by proper layout and shielding techniques the effect of interference noise can be nullified for a circuit [5]. On the other hand, the inheritance noise can be reduced and cannot be eliminated completely, thereby presenting a practical limit on the performance of electrical circuits and systems [5]. For example, in a RF front-end receiver the noise performance is determined mainly by the interaction between Low Noise Amplifier (LNA), Mixer and Local Oscillator (LO) and also the noise due to each of those individual circuits. To fully understand the influence of noise on the overall performance of the analog/RF design and meet the specification, it is necessary to model and verify all dynamics involved in the design. However, analog/RF designs face a setback in modeling and verification primarily due to:

- The use of deep-submicron processes that give rise to an exponential increase in the number of devices in a design, thereby, creating a need for accurate modeling that could capture the complex noise dynamics of analog/RF/digital interfaces at the component and behavioral levels for a full chip verification;
- High operating frequencies, process variations and environment constraints that make the design susceptible to noise, thereby making the verification unmanageable at the circuit level [20]; and
- In case of communication systems, designs are subject to different protocol/standards, thereby requiring a huge effort in modeling and verification that adhere to multiple functionalities [3].

Traditionally, circuit simulators are used to simulate and analyze the analog/RF designs that are described as a netlist in SPICE [11]. Unlike digital simulators, computer aided design (CAD) tools for analog/RF are not mature enough to handle complex designs thereby, forcing the designers to rely on experience, intuition, or inefficient simulation techniques to predict the performance. In addition, circuit simulators suffer from longer simulation run-times which may cause delays in the overall design and verification effort.

In recent years many researchers have worked around the problem of expensive simulation run-times by modeling the analog/RF designs at higher level of abstraction. However, with different types of noise sources (thermal, shot and flicker), the challenge faced by the designers is to choose the appropriate type of noise model without compromising on simulation run-times and accuracy.

The first step is to find an adequate model for analog/RF designs with noise. Unfortunately, the usual statistical analysis of stochastic processes does not allow designers to describe the random behavior of a system in time domain. In fact for a model based on linearization techniques for a time-invariant design, the assumption is that noise does not affect the operating points and the inputs are assumed to be periodic. As a consequence, these kind of models are only applicable for linear systems and are solved in general using frequency domain techniques. However, when the noise is large, the operating points vary due to nonlinearity and hence accurate results are only achieved through transient simulation, but

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suffer from longer simulation run-times. Due to the statistical behavior of the noise, we are interested in finding a statistical solution rather than a detailed response of the system, therefore we propose to use stochastic differential equations (SDE) [4] as an analog/RF noise model allowing designers to capture the statistical properties of the design in continuous-time. However, the challenge is to incorporate verification techniques that are suited for SDE based modeling.

Verification based on Monte-carlo methods [17] are commonly used to analyze any random systems. But, the method is inefficient because it lacks a structure that could characterize the drift and diffusion coefficients in SDEs. Moreover, it inherits the coverage limitation drawbacks from standard simulation methods. Alternatively, in recent years, formal and semi-formal methods have been advocated by many research groups and industries for analog and mixed signal verification [14]. In particular, monitoring techniques based on assertions have been shown to be effective in detecting violation of the design specification thereby avoiding exhaustive checking inherited by traditional circuit simulator and formal methods.

In this paper, we take this verification process a step further, by investigating the usefulness of monitors for analog/RF designs, especially in the presence of noise. We propose an assertion based verification methodology for monitoring noise in analog/RF designs modeled using SDEs. Our approach is illustrated on a nonlinear tunnel-diode and a Colpitts oscillator circuits in order to study the behavior in the presence of noise.

The rest of the paper is organized as follows: In Section II, we review the state-of-the-art in noise modeling and verification of analog/RF designs. In Section III, we outline the theory and modeling of analog/RF designs using SDEs. In Section IV, we introduce the proposed methodology for monitoring noise in analog/RF designs. Experimental results are illustrated in Section V, followed by discussions and conclusion in Section VI.

II. Related Work

In general, noise modeling and simulation are done either using harmonic balance frequency domain techniques or monte-carlo based time domain techniques. The former suffers from memory space problems, while the monte-carlo based technique suffers from expensive simulation run-times. But in recent years, several advances have been made in the area of noise modeling and verification of analog/RF circuits based on SDEs. For instance, in [15] the author performs an SDE based phase noise simulation in time domain using the circuit simulator *f*REEDA [8]. Though the phase noise is accurately predicted for a fairly large frequency range, their technique suffers from long simulation run-times without the mean to be able to detect undesired behavior. Similar work was conducted in [24], where second-order SDEs are used to simulate the phase noise in a submicron CMOS LC oscillator. In contrast, numerical integration methods for behavioral noise analysis have been reported by the authors in [2], [25]. This method proves to be accurate, but is unscalable to larger designs. A behavioral approximation of SDEs based on Euler-Maruyama method for an RL circuit is outlined by the author in [7] and the model is numerically simulated for analysis. A different analysis using model order reduction technique is introduced in [19] for noise modeling of linear time invariant systems (LTI) and simulated using MATLAB [13], but the model proves to be insufficient for time varying systems. A complete simulation based SDE noise analysis of a mixer is performed by the authors in [6] for calculating the optimum value of noise figure and conversion gain. The method provides an effective and accurate simulation result that could be incorporated into the transient analysis of circuit simulators, but suffers from expensive run-times. In summary, the above work emphasize the use of SDEs for noise modeling, but fail to extend them for developing verification methodologies. In contrast, we propose an assertion based verification technique for monitoring noise in an analog/RF circuit.

On the verification side, semi-formal methodologies have been presented by many researchers for analog and mixed signal (AMS) designs. The most prominent is the work presented in [16], where the authors proposed a PSL (Property Specification Language [1]) based *offline* methodology for monitoring the simulation of continuous signals. An approach using assertion based verification technique is also introduced in [9]. The authors use systems of recurrence equation (SRE) for modeling and *offline* based monitoring method for verification of analog and mixed signal systems. In contrast to *offline* based verification, the authors in [10] propose an *online* monitoring technique but, their method cannot support mixed system behavior and any practical property specification language. More recently in [26] the authors have used SREs to express PSL properties for AMS design. They present a tool, named C-SRE, which simulates AMS designs modeled with SREs, reads PSL properties and realizes the online monitoring.

Although there are several papers that target noise modeling and verification separately for analog/RF designs, none of them provides a common platform for noise modeling and monitoring. In this paper, we propose, to the best of our knowledge, the first unified methodology to model the noise of an analog/RF circuit based on stochastic differential equation (SDE) and verified it using assertion based verification technique.

III. Preliminaries

A. Stochastic Differential Equation (SDE)

An SDE is an ordinary differential equation (ODE) with stochastic process [4]. Given the probability space ω, a stochastic process with state space E is a collection $\{X_t;\ t \epsilon T\}$ of random variables X_t that take values in E for the parameter set T. If T is countable then the stochastic process is *discrete* else *continuous*. Due to statistical properties, a stochastic process can be used to define the randomness in an SDE, thus allowing designers to model the noise behavior of any continuous system. Noise in SDEs is incorporated as an uncorrelated *white gaussian noise* which can be thought of as the derivative of Brownian motion (or the Wiener process) [4].

Example. Consider the RL circuit as shown in Figure 1. The ODE describing the behavior of the RL circuit is given by

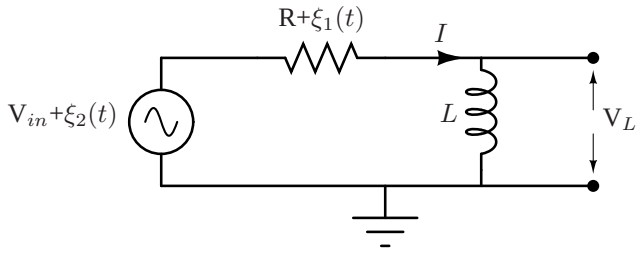

Fig. 1. Series RL Circuit [7].

$$L\frac{dI}{dt} + RI(t) = V_{in}(t), \quad I(0) = I_0 \tag{1}$$

where the resistance *R* and the inductance *L* are design parameters and $V_{in}(t)$ denotes the input source at any time *t*. Assuming white noise process at the input voltage source and at the resistor, we obtain the following

$$L\frac{dI}{dt} + (R + \alpha\xi_1(t))I(t) = V_{in}(t) + \beta\xi_2(t) \tag{2}$$

where $\xi_1(t)$ and $\xi_2(t)$ are two independent white noise processes, and α and β describe the amplitude of the noise. Considering $dW_1(t)$ and $dW_2(t)$ two uncorrelated Wiener processes representing ξ_1 and ξ_2, respectively, then Equation (2) can be written as:

$$L\frac{dI}{dt} + \big(R + \alpha\frac{dW_2(t)}{dt})I(t\big) = V_{in}(t) + \beta\frac{dW_1(t)}{dt} \tag{3}$$

Rearranging Equation (3), we have the corresponding SDE:

$$dI(t) = \frac{1}{L}\big(V_{in}(t) - RI(t) - \alpha dW_2(t)I(t) + \beta dW_1(t)\big) \tag{4}$$

Generally, SDEs cannot be solved using traditional mathematics for the steps of the transformation because the Wiener process is non-differentiable, instead we need special techniques such as *Itò* [4] and *Stratonovich* calculus [4]. However, there is not always a closed form solution for SDEs, hence researchers have looked for solving them numerically. The methods based on numerical analysis are reported in [18], which involve discrete time approximation in a finite time interval over the sample paths. Neglecting the errors due to numerical approximation, the simplest time discretization approach is based on *Euler-Maruyama* approximation [18] which we adopt in this paper.

Consider an *Itò* SDE in differential form

$$dX_t = a(X_t)dt + b(X_t)dW_t \tag{5}$$

where *a* and *b* are some functions of time and W_t is a Wiener process. Based on *Euler* approximation, Equation (5) can be written as:

$$X_{n+1} = X_n + a(X_n)\Delta_n + b(X_n)\Delta_n\Delta W_n \tag{6}$$

where for time step τ,

$$\Delta_n = \tau_{n+1} - \tau_n; \;\; \Delta W_{\tau n} = W_{\tau n+1} - W_{\tau n} \tag{7}$$

for *n=0,1,2.....N-1* with initial value $X_0 = x_0$; and for maximum *N* simulation steps.

The recursive method described by Equations (6) and (7) gives only an approximate solution and it is important to note that the solution is close to the *Itò* process [18]. The amount of deviation of the numerical solution is defined by the *absolute error* which satisfies the convergence properties. More accurate numerical methods such as *Milstein, Taylor, Runge-Kutta* that have strong and weak convergence are available in [4] for the numerical simulation of the analog/RF designs.

IV. Methodology

Figure 2 depicts the proposed methodology for run-time verification of assertions on noise effects. Thereafter, given an analog/RF design described as a system of *ODEs*, the idea is to include a stochastic process that describes the noise behavior. Since there are no functions/procedures that can automatically incorporate stochastic processes, we manually generate the *SDEs*. We then manually rewrite the *SDEs* based on the numerical technique described above. The numerical approximation of the design, along with the properties to be monitored, and the environment constraints (such as the amplitude of noise, etc.) are coded and simulated in MATLAB [13] as described later.

The analog/RF design is simulated within the given environmental constraints. This may include the amplitude of the noise, initial conditions of the circuit current and voltages. For instance, in case of the RL circuit described in Figure 1, α and β represent the magnitude of the noise which determines the deviation of the stochastic output from the deterministic one. The environment constraints are passed as a parameter to the design under verification during simulation.

An assertion is a piece of code that evaluates the outputs of the simulator and checks whether the property satisfies the design specification. If the property is satisfied, the monitor reports the satisfaction. Otherwise, the monitor can terminate the simulation using *exit* commands at the cycle when the violation occurs. The monitor could be as simple as observing a current or voltage, or could be more complicated, taking several signals, processing and then comparing them against the expected results. The monitors could be constructed so that signals could be observed in an *online* or *offline* fashion. While the online monitoring is more practical when simpler properties are needed to be verified and violations are identified as soon as they occur, offline monitors allow the verification of more complex properties but require the gathering of simulation results which can cost a lot of memory resources. In this paper, we extend the idea of monitoring analog mixed signal to the next level by developing assertions for monitoring noise in analog/RF designs. In the proposed methodology the monitors are simple finite state machines (FSM) constructed using *if-then-else* MATLAB constructs as described later.

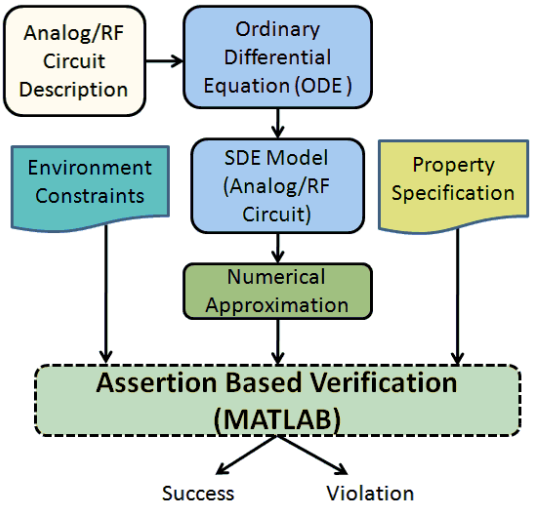

Fig. 2. SDE based Run-Time Verification

V. Experimental Results

We have applied the proposed methodology to several benchmark circuits, including a tunnel diode oscillator [23] and a Colpitts oscillator [12].

A. Tunnel Diode Oscillator

The circuit diagram of a tunnel diode oscillator is shown in Figure 3. The tunnel diode exploits a phenomenon called resonant tunneling due to its negative resistance characteristic at very low forward bias voltages. This means that for some range of voltages, the current decreases with increasing voltage. This characteristic makes the tunnel diode useful as an oscillator. The first step in noise analysis, is to identify and incorporate the sources of noise as a stochastic process in the SDE.

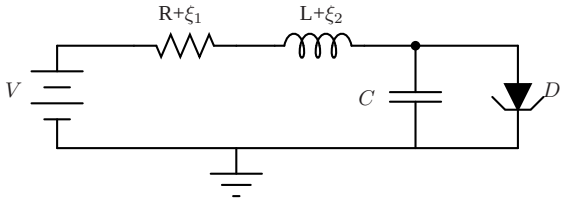

Fig. 3. Tunnel Diode Oscillator

$$\begin{aligned} \dot{V_C} &= \frac{1}{C}(-I_d(V_C) + I_{RL}) \\ \dot{I_{RL}} &= \frac{1}{L}(-V_{C1} - \frac{1}{G}I_{RL} + V) \end{aligned} \tag{8}$$

where $I_d(V_C)$ describes the non-linear tunnel diode behavior given by $I_d(V_c) = V_c^3 - 1.5 * V_c^2 + 0.6 * V_c$. For simplicity, we assume three noise sources, contributed mainly by the input voltage source *V*, the resistor *R* and the inductor *L*. We then derive the SDE model as described by Equation (9).

$$\begin{aligned} dV_C &= \frac{1}{C}(-I_d(V_C) + I_{RL})dt + (dW_{2t} + dW_{3t}) \\ dI_{RL} &= \frac{1}{L}(-V_C - RI_{RL} + V)dt + \frac{1}{L}dW_{1t} \end{aligned} \tag{9}$$

The first-order numerical approximation of the SDE model described by Equation (9) is derived as

```
% Initialization (for j=1)
IRL(1) = 0.04e-3;
Vc(1)  = 0.8;
W1(1) = sqrt(Delta)*randn;
W2(1) = sqrt(Delta)*randn;
W3(1) = sqrt(Delta)*randn;

% Calculation of Vc and IRL
for j = 2:N
dW1(j)= sqrt(Delta)*randn;
W1(j)= W1(j-1) + dW1(j-1);

dW2(j)= sqrt(Delta)*randn;
W2(j)= W2(j-1) + dW2(j-1);

dW3(j)= sqrt(Delta)*randn;
W3(j)= W3(j-1) + dW3(j-1);

Vc(j)= Vc(j-1)+ Delta*(1/C)*(-(Vc(j-1))^3
+ 1.5*(Vc(j-1))^2 -0.6*(Vc(j-1)) + IRL(j-1))
+ Delta*(W2(j-1)+W3(j-1));

IRL(j)= IRL(j-1) + Delta*(1/L)*(-Vc(j-1)
-(1/G)*IRL(j-1) + Vinput + W1(j-1));
end
```

Here W_1, W_2 and W_3 represent the Wiener processes depicting the noise in *V*, *R* and *L*, respectively. V_c represents the non linear behavior of the tunnel diode oscillator, N_{max} is a natural number representing the total simulation cycle, predefined before the start of the simulation, and *randn* represents any system generated random number for representing the Wiener process. *Delta* represents the simulation step-size that is required to provide a desired time resolution and accuracy for the numerical solution of the SDEs. The value of *Delta* depends on the type of the circuit and parameter of the circuit elements. I_{RL} represents the current through the inductor.

Property Observations

In general, for tunnel diode oscillation, the kind of properties we are interested to verify are: *Is the system behavior the same for the set of initial condition?* or *For which set of parameters values, the circuit oscillates or dies?* The properties that we verify in this paper are the oscillation and no oscillation for different circuit parameters shown in Table I.

TABLE I
Tunnel Diode Oscillator Parameters

Parameter	Property 1		Property 2	
	Without Noise	With Noise	Without Noise	With Noise
Conductance $(G)\Omega^{-1}$	2000e-3	2000e-3	5000e-3	5000e-3
Inductor (L) H	1e-6	1e-6	1e-6	1e-6
Capacitor (C) F	1000e-12	1000e-12	1000e-12	1000e-12
V_0 Volts	0.131	0.05	0.8	0.1
I_0 Amps	0.055	0.018	0.04e-3	0.002

Property 1: We verify that for the set of parameters given in Table I, there is no oscillatory behavior. The behavior in

question is stated as the bounded safety property, meaning for no oscillation property to be satisfied, if for the given simulation time step a certain threshold will not be reached then the property is violated thereby enabling a *violation signal*. The implementation of the assertion as a finite state machine (FSM) for verification of *no oscillation* property is shown in Figure 4.

The FSM has five states namely, *initialization*, *cycling*, *violation* & *cycling, error and stop simulation*. The maximum simulation time, N_{max}, and inputs like initial voltage, current and output violation are set in the *initialization* state. As soon as the simulation starts, the FSM goes to the *cycling* state and remains until $T < 3.8 * 10^5$ or $T > 5.5 * 10^5$, where the output voltage $V_c(t)$ is just reported and not observed for any violation. This is because, though the simulation is done from $T = 0$ to $T = N_{max}$, the *no oscillatory* property is verified for the bounded interval $T > 3.8 * 10^5$ to $T \leq 5.5 * 10^5$. As *T* becomes greater than $3.8 * 10^5$ it goes into the $violation\&cycling$ state where the property is verified for any violation, meaning if $V_C(t) < 0.6$, the property is satisfied or else the violation signal is asserted and the FSM enters into the *error* state where it remains there till $T \leq N_{max}$, and then goes to the *stop simulation* state.

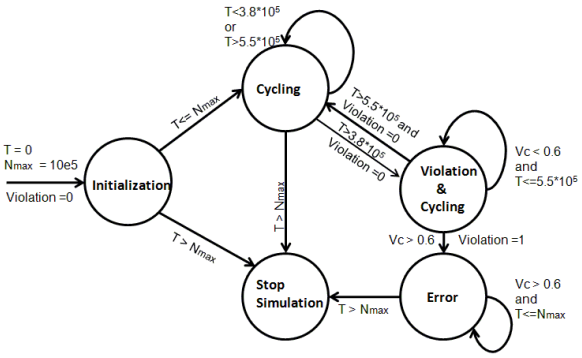

Fig. 4. Property 1 FSM

The results for the verification of Property 1 is shown in Figure 5. The results are obtained by simulating the numerical approximation of the SDEs and the assertion using MATLAB. For the given set of parameters and in a bounded region, the authors in [23] have verified the *no oscillation* property in the absence of noise based on abstract state machine model and ACTL [22] specification for verification. Moreover, the method assumes ideal resistor, capacitor, inductor and diode which is not true for real applications. However, the question that has to be answered is *For the given set of initial conditions and bounded region, how does the effect of noisy resistor, capacitor and inductor affect the oscillatory behavior of the tunnel diode oscillator?* meaning will the tunnel diode oscillator which has been proved to be stable and non oscillating produce the same stable result in the presence of noise?

First, we simulated the tunnel diode oscillator in the absence of noise and obtained a non-oscillating output as

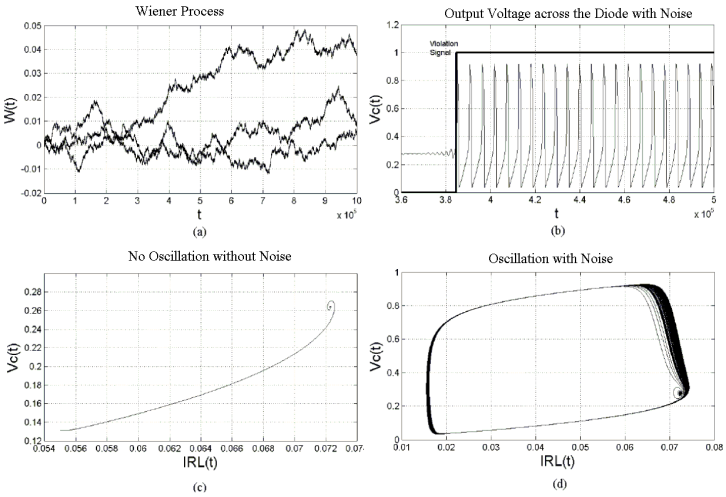

Fig. 5. Property 1 Simulation Result

shown in Figure 5 (c). The goal now is to show whether the property holds/violates in the presence of noise. The noise is modeled and simulated as a Wiener process as shown in the Figure 5 (a). From the simulation results bounded between $T = 3.8 * 10^5$ and $T = 5.5 * 10^5$ as shown in Figure 5 (b) and (d), we note that between $T = 3.7 * 10^5$ until $T = 3.8 * 10^5$, the output has an unstable oscillation, but at $T = 3.8 * 10^5$ the oscillator produces a stable oscillation thereby detecting a violation. The additive noise W_2 and W_3 in the voltage equation $V_c(t)$ causes the tunnel diode oscillator circuit to move to negative resistance region, thereby creating oscillation.

Property 2: We verify that for the set of parameters and initial conditions the tunnel diode produces a stable oscillation. The oscillation property can be understood as within the time interval [0, *T*] on every computation path, whenever the *Vc* amplitude will reach [0.9v, 1.0v], it will reach this value again until the simulation stops. The proposed monitoring technique based on *if-then-else* makes it difficult to detect oscillation, but can detect failure to oscillate. We show that within a bounded region, we prove whether the oscillation dies in the presence of noise, meaning, no oscillatory behavior, even though in the noiseless model it was proved to oscillate [23]. The implementation of the assertion as an FSM for verifying the absence of oscillation is shown in Figure 6. The details follow exactly like in Property 1 except that the bounded region for verification of *no oscillatory* behavior is between *T*=$3.0 * 10^5$ until *T*=N_{max}. The simulation results for the verification of Property 2 are shown in Figure 7. From the simulation results, we notice that the tunnel diode produces a stable oscillation in the absence of noise. However, in the bounded region from *T*=$3.0 * 10^5$ until *T*=$10.0 * 10^5$, the oscillatory behavior dies out in the presence of noise, thereby detecting a violation as shown in Figure 7(b). This shows that the noise has an adverse effect on the performance of the design under verification. Moreover, we demonstrated that, the oscillatory behavior which has been

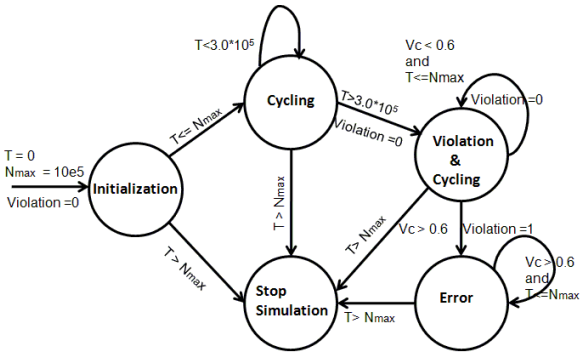

Fig. 6. Property 2 FSM

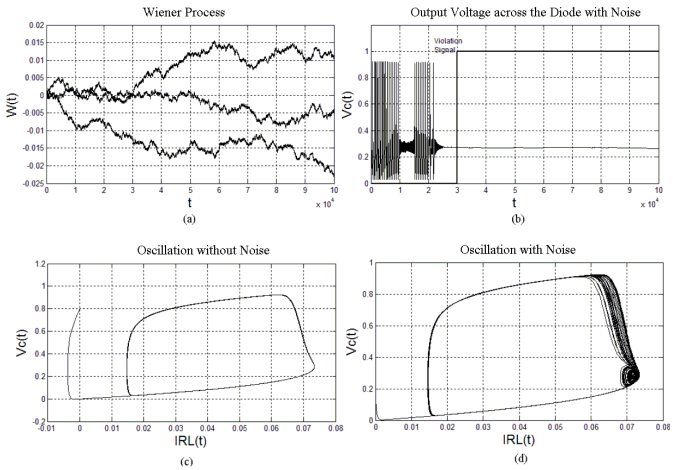

Fig. 7. Property 2 Simulation Result

proved in [23] does not hold under noisy conditions, thereby making our methodology robust in detecting errors.

B. Example 2: Colpitts Oscillator

The circuit diagram for a MOS transistor based Colpitts oscillator is shown in Figure 8. For the correct choice of component values the circuit will oscillate. This is due to the bias current and negative resistance of the passive tank.

For simplicity, we assume the noise only from the passive elements, while the noise from the MOS transistor is ignored. The first step in noise analysis, is to identify and incorporate the sources of noise as a stochastic process in the SDE. The simplified system of equations that describe the behavior of the Colpitts oscillator is given by:

$$\begin{aligned} \dot{V}_{C1} &= \frac{1.2-(V_{C1}+V_{C2})}{RC} + \frac{I_L}{C} - \frac{I_{ds}}{C} \\ \dot{V}_{C2} &= \frac{1.2-(V_{C1}+V_{C2})}{RC} + \frac{I_L}{C} - \frac{I_{ss}}{C} \\ \dot{I}_L &= \frac{1.2-(V_{C1}+V_{C2})}{L} \end{aligned} \tag{10}$$

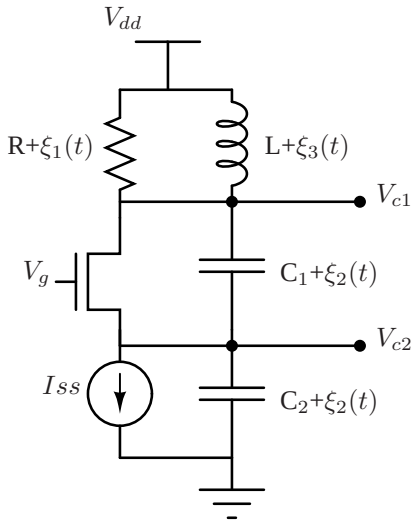

Fig. 8. Colpitts Oscillator

where

$$I_{ds} = \begin{cases} 0 \text{ if } V_{C2} > 0.3 \\ K\frac{W}{L}((0.3-V_{C2})(V_{C1}) - 0.5(V_{C1})^2) \text{if } V_{C1}+V_{C2} < 0.3 \\ K\frac{W}{L}(0.3-V_{C2})^2 \text{ if } V_{C1}+V_{C2} \geq 0.3 \end{cases}$$

The first-order numerical approximation of the SDE model described for the Colpitts oscillator circuit is derived as

```
% Initialization (for k=1)
IRL(1) = 0;
Vc(1)  = 0;
W1(1) = sqrt(Delta)*randn;
W2(1) = sqrt(Delta)*randn;
W3(1) = sqrt(Delta)*randn;

% Calculation of Vc1_2, Vc2_2 and IL_2
for k = 2:N
dW1(k) = sqrt(Delta)*randn;
W1(k)  = W1(k-1) + dW1(k-1);

dW2(k) = sqrt(Delta)*randn;
W2(k)  = W2(k-1) + dW2(k-1);

dW3(k) = sqrt(Delta)*randn;
W3(k)  = W3(k-1) + dW3(k-1);

Vc1_2(k)= Vc1_2(k-1)+ Delta*(1.2-(Vc1_2(k-1)
+ Vc2_2(k-1)))/(R*C)+ Delta*(IL_2(k-1)/C)
- Delta*(Ids_2/C) + alpha*(W1(k-1)+W2(k-1));

Vc2_2(k) = Vc2_2(k-1)+ Delta*(1.2-(Vc1_2(k-1)
+ Vc2_2(k-1)))/(R*C) + Delta*(IL_2(k-1)/C)
- Delta*(Iss/C)+ alpha*(W3(k-1)+ W2(k-1));

IL_2(k) = IL_2(k-1) + Delta*(1.2- (Vc1_2(k-1)
+ Vc2_2(k-1)))/L1 +alpha*W3(k-1);
end
```

Here W_1, W_2 and W_3 represent the Wiener processes depicting the noise in R, C and L, respectively. I_{ds} represents the drain-to-source current, α represents the amplitude of the noise, V_{C1}, V_{C2} represents the output voltage across the capacitors C_1 *and* C_2, respectively, and N is a natural

number representing the total simulation cycle, predefined before the start of the simulation, and *randn* represents any system generated random number for representing the Wiener process. *Delta* represents the simulation step-size, while I_L represents the current through the inductor and I_{SS} represents the bias current.

Property Observations

The property that we are interested in analyzing is *whether for the given parameters and initial conditions the circuit will oscillate?* The simulation results in Figure 10 show the variation of output voltages Vc_1 and Vc_2 with and without noise. The property that we verify in this paper is the no oscillation for different circuit parameters shown in Table II.

TABLE II
COLPITTS OSCILLATOR PARAMETERS

Parameter	No Oscillation Property	
	Without Noise	With Noise
Resistor (R) Ω	400	400
Inductor (L) H	3e-6	3e-6
Capacitor ($C_1 = C_2 = C$) F	20e-12	20e-12

The behavior in question is stated as the bounded safety property, meaning for the given simulation time step oscillation will not occurs if the current cannot exceed a certain threshold. For the no oscillation property to be satisfied, the

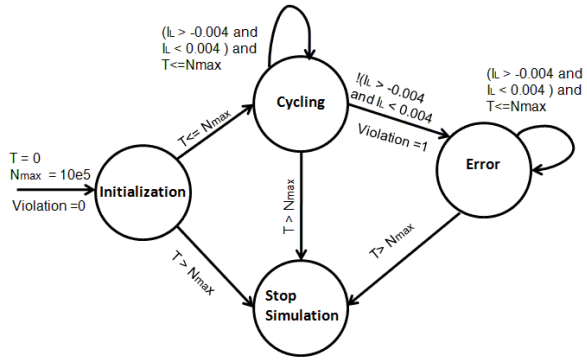

Fig. 9. No Oscillation Property FSM

current through the inductor I_L should be bounded within $[-0.004, 0.004]$. If verified to true, the property is satisfied else a violation signal is enabled. The implementation of the assertion as a finite state machine (FSM) for verification of no oscillation property is shown in Figure 9.

The FSM has four states namely, *initialization*, *cycling*, *error and stop simulation*. The maximum simulation time, N_{max}, and output violation are set in the *initialization* state. As soon as the simulation starts, the FSM goes to the *cycling* state and remains until $T \leq N_{max}$ and there are no violations observed. If the inductor current crosses the bounded threshold, the FSM asserts the *violation* signal and goes into the $error$ state where it remains there till $T \leq N_{max}$ and then goes to the *stop simulation* state.

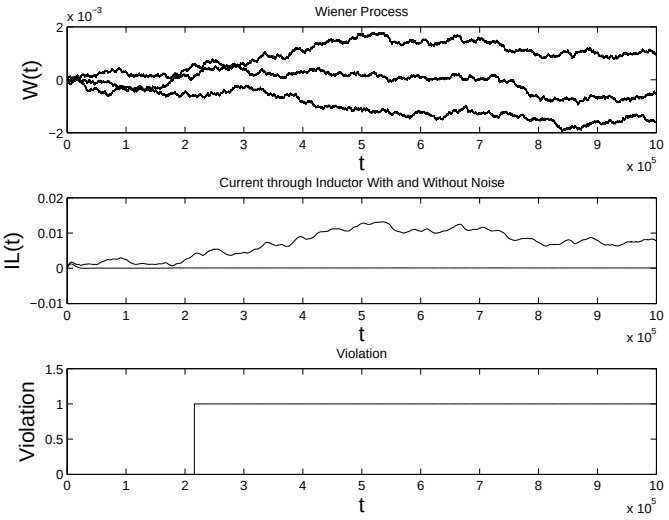

Fig. 10. Simulation Result of Colpitts Oscillator

From the simulation results, we notice that the Colpitts oscillator does not oscillate in the absence of noise. However, in the bounded region from T=$2.0 * 10^5$ until T=$10.0 * 10^5$, the current increases in the presence of noise, thereby detecting a violation. This is mainly due to the additive noise W_3 in the inductor current equation, thereby causing the current to increase. This shows that the noise has an adverse effect on the performance of the design under verification.

Discussion

In general, the simulation results are derived for one particular set of Wiener process, this is because the values of the Wiener process depends on the random number generator of the system and so we may find different sets of W_1, W_2 and W_3 during each simulation run. Therefore we conclude that, for this particular set of parameter values of W_1, W_2 and W_3 and initial conditions the properties in the tunnel diode and Colpitts oscillators are violated, but, we can get a different set of values for the Wiener processes for which the property holds. Hence, the verification has to be done for multiple trajectories before concluding the correctness of the design.

VI. CONCLUSION

In this paper, we have presented a practical assertion based verification methodology for noise in analog/RF designs. The approach is based on modeling the noise using SDEs and numerically simulating the model in MATLAB environment, and monitor the property of interest in an online fashion, thereby avoiding large simulation run-times. We have used the methodology to verify the oscillatory behavior of a tunnel diode oscillator and Colpitts oscillator. We showed that the properties that are satisfied without noise, have failed in the presence of noise, thereby proving that the proposed verification environment is efficient in finding bugs. This process is much more reliable than manual (visual or textual) inspection of simulation traces which will cost lots of time.

Due to the statistical property of the noise, we plan to develop monitors based on *Markov chains* which can be considered as finite state machines. Given the *present state*, future states are independent of the past states and the future states will be reached based on probabilistic process instead of a deterministic one. Our proposed approach currently is limited to linear SDEs and we would like to investigate higher order designs such as $\Delta\Sigma$ modulator and complex circuits like phase locked loops (PLL) that involve the use of second order SDEs with one-dimensional and multi-dimensional noise.

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