Cross Recurrence Verification Technique for Process Variation-Resilient Analog Circuits

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***Abstract*—This paper explores the impact of device process variations on the performance of analog circuits. We propose a new verification approach called Cross Recurrence Verification (CRV). Circuit output similarities between an ideal circuit that has parameters set to the nominal values and a non-ideal circuit with process variation due to $65nm$ fabrication process are computed. CRV is used to find the percentage of recurrence and the longest common output subsequence that matches the output subsequence of an ideal circuit. The performed analysis showed the potential of this novel technique to enhance/improve the verification process of Analog circuits. The proposed approach is illustrated on a five stage ring oscillator. The obtained results demonstrate the robustness, accuracy and flexibility of our methodology.**

I. Introduction

As Integrated Circuit (IC) technologies aggressively scaled to lower feature sizes and circuit applications moved to higher frequency bands, analog designers face new challenges in addition to a host of physical and functional constraints. Large scale process variability in modern circuits has become a major concern in the design of many analog circuits. In sharp contrast to the scaling down of modern device feature sizes, variability in the process parameters expand significantly exhibiting different device characteristics. In particular, uncertainties in transistor sizes and threshold variation are pervasive and deeply impact the functionality of a circuit which makes its verification extremely difficult. For instance, shrinking the

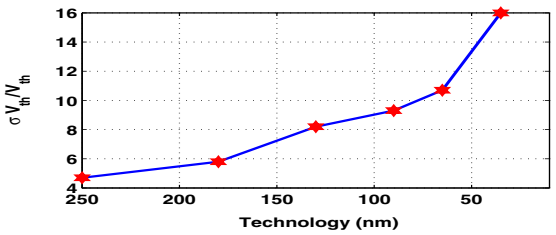

Fig. 1. Transistor threshold voltage standard deviation for different CMOS technologies [1]

to still commit non-optimal analog designs to the foundry. Hence, ensuring a robust operation of these non-optimal designs in the presence of process variation disturbance is an essential requirement that dictates careful verification of analog circuits. Therefore, empowering designers with new tools and techniques in order to tape out circuits that withstand process variation while meeting strict specifications are highly required. Subsequently, new verification techniques become the frontier research topic in recent years for design and manufacturing of high-performance VLSI circuits. Traditionally, Monte Carlo simulation techniques are used to verify circuits as well as behavioral models of analog designs. Based on repetitive simulations, Monte Carlo simulation permits the evaluation of substantive design properties as well as the statistical estimation of circuit parameters. To do so, this approach needs a pre-specified underlying distribution, mainly uniform, normal, or log-normal to describe the random variables of process variation effects. Hence, a wrong distribution assumption leads to a possibility of outright wrong results [2]. In addition, because the accuracy of this method is directly related to the number of simulation runs, this method results in long simulation times, and it is unlikely that the worst-case mismatch scenario is stumbled across [3]. Techniques based on formal methods, such as reachability analysis [4] have been successfully used to verify safety properties in simple analog circuits, such as the tunnel diode oscillator. Such reachability analysis approaches are still in their infancy and find only approximations to the sets of possible state-space trajectories. Therefore, complementary techniques that can examine the error growth at run-time are sought after. In [5], the authors used a pattern matching technique called Longest Closest Common Subsequence (LCSS) to find the longest and closest circuit output subsequence that matches with the subsequence of an ideal circuit. To demonstrate the effectiveness of their approach, the authors verified oscillation properties in a MOS transistor based Colpitts oscillator. However, this circuit has been reported to exhibit chaotic behavior [6] and therefore its verification in the phase space would be more adequate.

This paper tries to address some of the shortcomings of the above approaches, by automatically ensuring the correctness of analog circuits in the presence of process variation using the concept of cross recurrence not in the time domain but alternatively in the phase domain. We propose a novel approach to verify the impact of process variation on analog circuits performance. By deriving some quality parameters, mainly percentage of recurrence and the longest common diagonal line, our approach will serve as a guideline for designers to select the "good" circuits.

The rest of the paper is organized as follows: In Section

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II, we detail the proposed Cross Recurrence Verification approach. Section III provides an overview of the proposed methodology. Experimental results for the verification of CMOS ring oscillator oscillation frequency are reported in Section IV. Section V summarizes the contributions of this paper and provides future work hints.

II. Cross Recurrence Verification (CRV)

The Cross Recurrence Quantification Analysis (CRQA) [7] technique is a powerful method to study dynamical systems. It has been used in various disciplines such as health sciences and financial systems. However, to the best of our knowledge there were no previous applications of CRQA for circuits verification. In this section, we present a variant of CRQA called Cross Recurrence Verification (CRV). The implementation of the CRV technique is described in Algorithm 1. Given two sequences of analog circuit outputs $X_{ideal} = \{X^1_{ideal}, X^2_{ideal}, ..., X^M_{ideal}\}$ and $X = \{X^1, X^2, ..., X^N\}$, the idea is to study the similarities (recurring properties and patterns) of these two sequences in the phase space trajectories. We denote X_{ideal} the output sequence of an ideal circuit and X the output sequence of the non-ideal circuit. To compute the similar patterns between these two circuits outputs, a tolerance parameter called radius threshold ϵ is defined. This tolerance parameter specifies the allowable deviation difference in terms of Euclidean distance between two circuit outputs to be considered recurrent (i.e, same output value/state). To derive the matching quality between these two sequences, CRV consists of two main steps as shown in Figure 2.

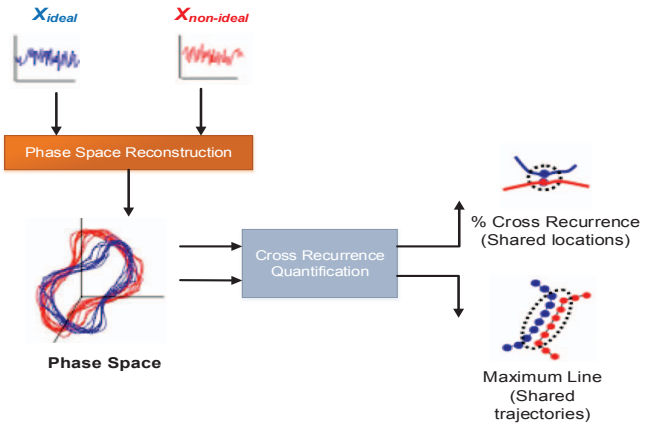

Fig. 2. CRV Concept

The first step involves overlaying delayed copies of the circuit output for each sequence separately (lines 4-7). The embedding lag τ (line 4) and the embedding dimension d_e (line 5) are computed using the Mutual Information function (*MI*) and the False Nearest Neighbours (*FNN*) function, respectively. Thereafter, the algorithm generates the different delayed copies of the output $X(t + m\tau), \forall m \in [1, d_e]$ by introducing multiple lags (lines 6 and 7).

The second step involves the computation of the pattern measures (lines 8-15). A cross recurrence matrix CR is

Algorithm 1 CRV Algorithm

Require: X_{ideal}, X, ϵ
1: $N \leftarrow length\ (X)$
2: $M \leftarrow length\ (X_{ideal})$
3: $N_c \leftarrow min(N, M)$
4: $\tau \leftarrow\ MI(X_{ideal})$
5: $d_e \leftarrow\ FNN(X_{ideal}, \tau)$
6: $Y_{ideal} \leftarrow Delay\_vector(X_{ideal}, d_e, \tau)$
7: $Y \leftarrow Delay\_vector(X, d_e, \tau)$
8: **for** $i = 1 \rightarrow N_c$ **do**
9: **for** $j = 1 \rightarrow N_c$ **do**
10: $CR(i, j) \leftarrow \Theta(\varepsilon - \|X_{ideal}(i) - X(j)\|)$
11: **end for**
12: **end for**
13: **for** $l = 1 \rightarrow N_l$ **do**
14: $p^{\epsilon}(l) \leftarrow Compute\_diagonal\_line\_lengths(CR)$
15: **end for**
16: $RR \leftarrow \frac{1}{N-k} \sum_{j-i=k} CR(i, j)$
17: $L_{max} \leftarrow max(p^{\epsilon})$
18: **return** RR, L_{max}

computed. It locates the recurrent points at coordinates (*i,j*) whenever similar phase space behaviour occurs on both circuit output sequences $X(i)$ and $X_{ideal}(j)$. In other words, it checks if the phase space trajectories of $X(i)$ at time i and $X_{ideal}(j)$ at time j fall within the predefined radius threshold ϵ (lines 8-12). This can be described by the following equation:

$$CR(i, j) = \begin{cases} 1 & \text{if } \|X(i) - X_{ideal}(j)\| < \varepsilon \\ 0 & \text{else} \end{cases} \quad (1)$$

The patterns between the two output sequences is revealed by diagonal lines in the recurrence matrix. For instance, these diagonal lines represent periods in one output trajectory that follow similar parallel behavior to those in another output. The closer the two outputs are, the more diagonal lines occur in the recurrence matrix. Subsequently, the frequency distributions of the diagonal lines lengths in CR are computed for each diagonal parallel to the main diagonal $CR(i - j = k)$ for k equal to a constant. Finally, the interplay between the two circuits outputs is characterized by two measures:

1) The recurrence rate RR which reveals the percentage of matching (i.e., the probability of the occurrence of similar state) in both circuit outputs.
2) The longest diagonal line L_{Max} that represents the longest uninterrupted period of time that both circuits stay attuned.

III. Proposed Methodology

Figure 3 depicts the overall proposed verification methodology based on the CRV technique to account for process variation in analog circuits. Given an analog design description (topology), a system of Ordinary Differential Equations (ODEs) is generated to describe the behavior of the circuit. For each technology, vendors create a library of devices with different corners that describe process variations of these devices.

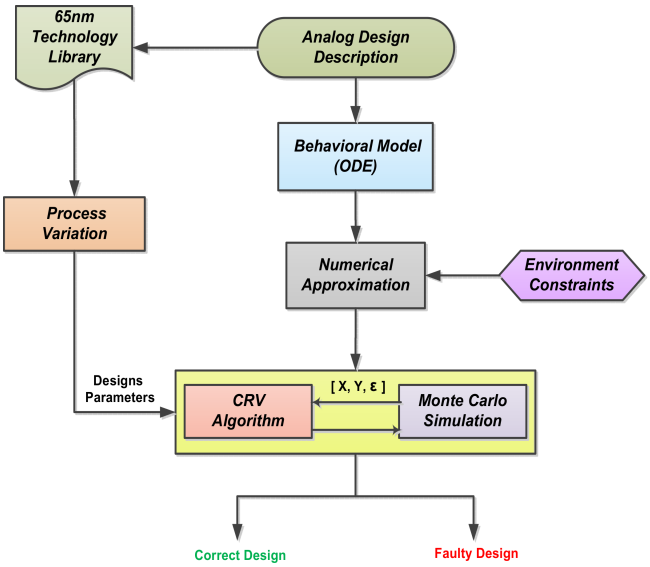

Fig. 3. Overview of the Proposed Verification Methodology

In our proposed methodology, circuit parameters are derived from a Gaussian distribution with standard variation σ defined by a $65nm$ process. The ODE model, process variation, and the environment constraints (i.e., simulation time, initial condition of current and voltage nodes) are evaluated using Monte Carlo simulation in a MATLAB simulation environment. We then generate two sets of sequences. One considered to be the sequence of an ideal circuit X and the other the sequence Y of a non-ideal circuit which exhibits process variation. These two sequences are verified using the CRV technique for the radius threshold ϵ. Based on the computed percentage of recurrence and maximal diagonal line, we can decide if the non-ideal circuit output exhibits similar/dissimiar behavior to the ideal one. Our methodology forms a novel approach for the evaluation of the impact of process variation on the analog circuit performance. It so allows the designer to decide whether an analog design is correct or faulty/defective.

IV. Experimental Results

In this section, we report the results of the application of our methodology in a ring oscillator. We used the CRV technique to verify that the oscillation frequency is within a specified tolerated range. All computation and circuit models were performed in a MATLAB environment and were run on a 64-bit Windows 7 server with 2.8 GHz processor and 24 GB memory.

A ring oscillator is comprised of an odd number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the circuit must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of $\frac{p}{n}$, where n is the number of delay stages. The methodology described in the preceding section is now applied to a five stage ring oscillator under process variation in transistor widths and threshold voltages. We choose this oscillator because it is commonly used because it has a small size, easy integration, multi-phase outputs, and a wide oscillation range. The schematic of the ring oscillator is shown in Figure 4. To model the influence of the interconnect circuitry, an additional load capacity C is used. Besides, a ratio of $W_p/W_n \simeq 2.5$ is chosen to compensate for the poorer performance of the p-MOS transistor so they achieve equal noise margins [8].

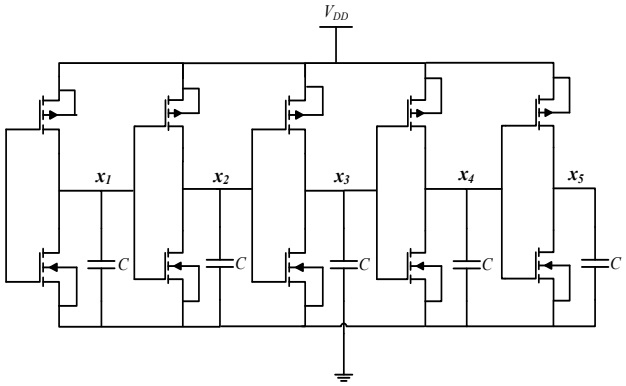

Fig. 4. Five Stage Ring Oscillator Schematic

The first step in the CRV approach is to generate the sets of sequences (ideal and non-ideal) for different process parameters. The circuits dynamics can be described by these ODEs:

$$\begin{aligned} \frac{dx_1}{dt} &= -\frac{1}{C}(I_n(x_n, x_1, gnd) + I_p(x_n, x_1, V_{DD}) \\ \frac{dx_i}{dt} &= -\frac{1}{C}(I_n(x_{i+1}, x_i, gnd) + I_p(x_{i+1}, x_i, V_{DD}),\ \forall i \in [2,5] \\ V_{out} &= x_5 \end{aligned} \tag{2}$$

The property of interest that we want to verify is: *"For a given set of parameters, whether the circuit will oscillate at 0.8 GHz with a tolerance bound of 50MHz ?"*.
Figure 5 depicts the simulated output of the ring oscillator in ideal conditions.

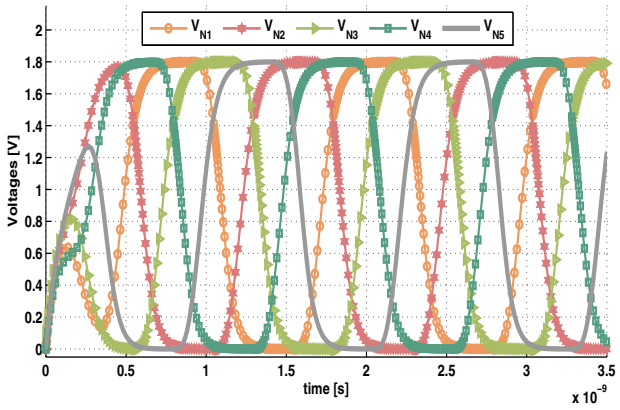

Fig. 5. Five Stage Ring Oscillator Outputs

We conducted the verification of 1000 Monte Carlo trials for three different process variation scenarios and for the simulation parameters given in Table I. The number of designs that satisfy the tolerated frequency of oscillation out of the total circuits generated (1000) are reported in Table II for different radius thresholds ϵ.

For a tolerance level of 0.1%, the output of the ideal ring oscillator (under nominal process parameter values) is within a $\pm 0.1\%$ radius of range of the non-ideal circuit output. It is apparent from rows 2-4 of Table II that increasing the tolerated radius increases the percentage of recurrence which induces a smaller number of faulty designs. It can also be noticed that the threshold voltage variation due to 65nm process (column 2) impedes more the oscillation frequency than the variation in the transistors width (both NMOS and PMOS).

TABLE I
SIMULATION PARAMETERS

Parameter	Value
$\sigma Vth/Vth$	10.6
W_n	10% variation
W_p	10% variation
d_e	3
τ	31

TABLE II
OSCILLATION VERIFICATION RESULTS

Tolerance (ϵ)	PV in V_{th}	PV in W_{n_i}	PV in W_{p_i}
0.1%	658	793	772
0.5%	702	815	859
1%	754	845	891

The percentage of recurrence points between the output subsequence of the ideal circuit and the circuit outputs under process variation in the threshold voltage V_{th}, NMOS transistor width W_n and PMOS transistor width W_p are shown in Figure 6.

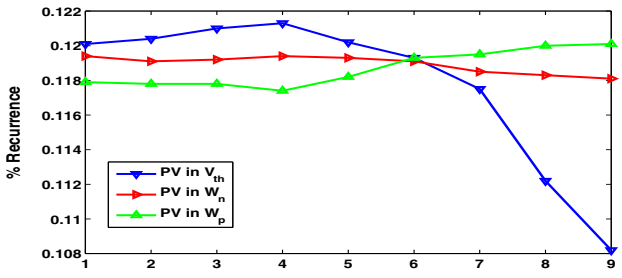

Fig. 6. Variation of the Percentage of Recurrence

In Figure 7, we show the longest common output subsequence that matches the output subsequence of the ideal circuit to the outputs under process variation for the same scenarios.

Both the percentage of recurrence and the maximal common line confirm the results reported in Table II. In fact, they both decrease significantly while varying the design parameters, especially in the case of threshold voltage variation.

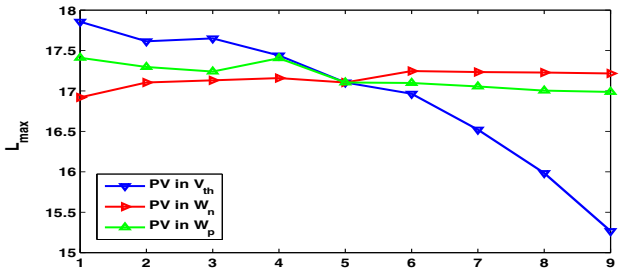

Fig. 7. Variation of the Maximal Diagonal Line

V. CONCLUSION

This paper presents a methodology based on cross recurrence verification to account for process variation in analog circuits. The approach is based on modeling the circuit at the behavioral level, and then integrating parameter variation in order to find the maximal common subsequence and the percentage of recurrence for a predefined radius threshold. These two measures can be used to estimate in terms of percentage the closest simulation trace that matches the simulation trace of the ideal circuit. The efficiency of our approach is illustrated on a Ring oscillator for $65nm$ fabrication process. The obtained results showed that a variation in the threshold voltage has the most tremendous effect in the oscillation frequency of a five stage Ring oscillator. The main advantage of the proposed methodology are robustness and its suitability for test automation. It is also readily extendable to other circuits architectures.

Worthwhile future work includes:(1) applying speed-up techniques for the cross recurrence computations; (2) extending the simulation step size to handle varying step-sizes to consider designs that are simulated by two different simulators with different step sizes; and (3) applying the methodology to more complex designs to assess its scalability.

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