A Statistical Approach to Probe Chaos from Noise in Analog and Mixed Signal Designs

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***Abstract*—Chaotic circuits have gained increasing attention in many engineering applications. Qualitative measures such as Lyapunov Exponent (LE) are the most common methods for identifying chaotic behavior. However, the use of these measures is limited due to the short output signal length and its contamination by noise. In this paper, we propose a novel methodology for modeling and detecting chaotic vs stochastic behavior in AMS designs. First, the design is modeled using a system of recurrence equations for analog and digital parts. Second, a surrogate generation method is performed. The obtained surrogates are a typical realization of the circuit output under the hypothesis that the circuits exhibits noise. Next, hypothesis testing with Gaussian Kernel measure as test statistic is conducted over these surrogates and the original circuit output to statistically assess the circuit behavior. The effectiveness of the proposed methodology is illustrated on several AMS circuits such as PLL or Colpitts oscillator. The obtained results show sufficient improvements over the existing methods. For instance, comparing with the LE method, our approach is an order of magnitude faster and provides a more accurate detection of the chaotic circuit behavior.**

I. Introduction

Chaotic circuits have potential applications in various fields such as communication [1], signal processing [2], and neural networks [3]. This is mainly because they present an unpredictable behavior that resembles noise with a broadband spectrum, so they can be deployed in encryption and random noise generation. Chaos can also be used to enhance Analog and Mixed Signal (AMS) circuits performance such as reduction of idle channel tones and pattern noise in Σ-Δ modulators [4] and stabilization of PLL by broadening its capture range [5]. Nevertheless, due to the nanometer-scale technologies, AMS designs manifest large scale process variations that cannot be reduced by foundries. This deviation in the geometrical and electrical device parameters can compromise the circuit's usefulness. Thereby, it might behave chaotically instead of periodically on a parameter change. This will affect the circuit performance (e.g., PLL locking, circuit stability, etc.) and consequently cause design failure. Experiments showed that in specific operation conditions (i.e., circuit parameter, initial conditions, and input signals) even remarkably simple nonlinear circuits can exhibit chaotic behavior [6].

When irregularity is observed in an AMS design output, designers assumes that the circuit exhibits stochastic noise which is stubbornly present in such designs. However, this could emerge from purely deterministic chaotic nonlinear circuit model. Because noise detection is a contentious issue for designers and there is a lack of efficient noise verification tools in AMS designs, a chaotic circuit could be analyzed to be noisy erroneously. It is fundamental therefore to thoroughly investigate and append the real source of an aberrant circuit behavior. To this end, there is a pressing need for handy chaos detection tools in AMS designs. Such tools can be used to probe the circuit dynamics at early stage and so assess the observed behavior (chaotic or stochastic) of the design.

In this paper, we propose a novel statistical verification methodology of AMS designs behavior, mainly chaotic and noisy dynamics. To speed up the verification runtime, the analog and digital components of the AMS circuit are modeled in a unified environment. The behavior of the circuit is described as function of the preceding state variables terms using Extended-System of Recurrence Equations (E-SRE) [7]. We then elucidate the intended property to be verified within the ambit of a null hypothesis H_0. Thereafter, we generate several artificial output of the circuit called surrogates. The generated surrogates should comply with the property being verified H_0 while preserving some features of the real circuit output. A discriminating statistic, namely the Gaussian Kernel measure, is then conducted for the original circuit output and all the generated surrogates. If the computed original output and surrogates statistics are significantly different, hypothesis testing technique reports a rejection of the null hypothesis H_0. As a consequence, we conclude that the circuit dynamic does not comply with its property.

The remainder of this paper is organized as follows: Related work is discussed in Section II. Section III provides an overview of the proposed methodology. Experimental results for the analysis of chaotic features on a Colpitts oscillator circuit, a third order Σ-Δ modulators and, a Phase Locked Loop are reported in Section IV. Section V summarizes the contributions of this paper and provides future work hints.

II. Related Work

The study of chaotic features in electronic circuits is the subject of an extensive research. Chaos detection is complicated by the lack of an accepted formal definition of chaos. For instance, despite the fact that chaotic features have been observed in Σ-Δ modulators, no literature provides satisfyingly rigorous proof of the presence of chaos in such circuits for orders higher than two [8].

978-1-4799-8719-1/15 $31.00 © 2015 IEEE
DOI 10.1109/ISVLSI.2015.101

To demonstrate the chaotic behavior of electronic circuits, qualitative metrics such as bifurcation diagrams have been proposed. This measure permits to visualize the different behaviors of the system as parameters change. Visualizing such diagram for high dimensional systems is very difficult and resources hungry. The use of qualitative methods, namely Lyapunov Exponent measure [9], is another paradigm that has been adopted to quantify chaos. It indicates the average rates of convergence or divergence of nearby trajectories. A positive exponent implies divergence and is indicative of chaotic dynamics while a negative one implies convergence and is said to be periodic.

Lyapunov Exponent is defined as a limit when time t approaches infinity (Equation (1)), one encounters fundamental difficulties using it for a circuit simulated for a limited time.

$$\lambda_i = \lim_{t\to\infty} \frac{1}{t} ln|\sigma_i(t)|, \forall i \in [1, .., n] \quad (1)$$

Where $\{\sigma_i\}_{i=1}^{n}$ are the eigenvalues of the Jacobian matrix of the circuit. This technique is hampered by technical issues related to the signal length and its contamination by noise (known as Perron effects); Hence, direct application of this measure on the circuit output might be inappropriate. To circumvent these shortcomings, we present, to the best of our knowledge, the first methodology to statistically investigate determinism in apparently stochastic AMS design behavior. Unlike the Lyapunov Exponent measure [9], the proposed methodology can also be adopted for circuit level AMS circuits outputs.

III. Proposed Methodology

An overview of our proposed methodology to statistically probe the dynamics (deterministic vs stochastic) of AMS designs is shown in Fig. 1. The AMS circuit behavior is modeled as a System of Recurrence Equations (SREs) that describes its behavior with/without noise. Recurrence equations are the discrete version of an analog differential equations. For the discrete components, the SREs are extended to E-SRE [7] by expressing them with *if-else* logical formulas as follows:

$$X_i(n) = f_i(X_j(n-\gamma)), \forall i, j, n \in \mathbb{Z} \quad (2)$$

where f_i is a generalized *If-formula*. In this work, we are considering only thermal noise excitation that adheres to a Gaussian distribution with mean m, and standard deviation σ. The obtained model is evaluated for specific environment constraints, namely the initial values of the voltage and current state variables and simulation parameters (such as the total simulation time, and the simulation step size). Thereafter, we elucidate the property of interest ($\mathcal{P}$) that the circuit should comply with. The property to be verified in this paper can be phrased as follows: "*Is the observed random like behavior of the AMS design due to noisy or chaotic behavior?*". Hence, we define a null hypothesis, denoted by H_0, which assumes that the circuit exhibits stochastic noise and an alternative hypothesis H_1 that assumes the circuits to be purely deterministic. To verify the above mentioned hypotheses, the idea is to generate artificial circuit outputs called surrogates that are realizations

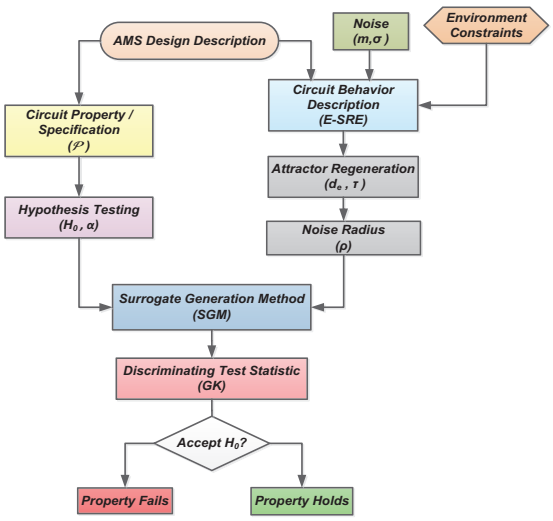

Fig. 1. Proposed statistical behavioral verification methodology

of what would the circuit output be if it was consistent with the property $\mathcal{P}$. Hence, these surrogates serve as a useful model against which to verify the real circuit output. They are carefully constructed from the circuit output so as to be free from any chaotic process while preserving some features of the original output.

To do so, we appeal to a different mathematical representation of the circuit behavior known as phase diagram in the nonlinear system theory. A phase diagram displays the circuit variables against each other and leaves time as an implicit dimension not explicitly graphed. The subset of this phase space toward which the circuit tends to evolve regardless of the initial conditions is called an attractor. This attractor will be used to predict the chaotic dynamics of the AMS circuit in order to consider them in the surrogates generation later. We applied the non uniform embedded window [10] and the false nearest neighbor method [11] for establishing optimal embedding parameters (d_e, τ) for the attractor reconstruction from the circuit output as depicted in Fig. 1. Thereafter, we determine the noise radius ρ that is the amount of noise that will obliterate the attractor of the surrogates. The best selection of this parameter is very important for the accuracy of the results. ρ is computed according to the suggestions in [12]. These parameters (d_e, τ, ρ) together with the hypothesis H_0 will be passed to the Surrogate Generation Method (SGM). A number of surrogates N_S will be generated using this method (more details will be given later in Section III-A). Those surrogates must preserve the coarse deterministic features of the real output (such as periodicity) while satisfying the null hypothesis H_0. Therefore, chaotic structure by fine scale dynamics will be altered by random noise with level ρ. To verify the AMS circuit behaviors, we perform hypothesis testing technique for a given confidence level α in order to derive the acceptance region for the noisy behavior expressed with the null hypothesis H_0. The acceptance region concludes that if the original circuit output test statistic is located outside

this region, H_0 is rejected. In other words, hypothesis testing approach reports a significant difference between the original output and its surrogates in term of Gaussian Kernel (GK) measure (see Section III-B for more details). The rejection of the null hypothesis implies the acceptance of the alternative hypothesis H_1 that the circuit behavior exhibits chaos.

A. Surrogate Generation Method

We extend the Pseudo Periodic Surrogate (PPS) method, developed first in [12] to study dynamics of human electrocardiogram (ECG), to verify AMS circuits behavior.
Algorithm 1 illustrates the surrogates generation procedures in order to verify aberrant behaviors of AMS designs described as Extended-System of Recurrence Equations (E-SREs).

Algorithm 1 Surrogate Generation Algorithm

Require: E-SRE(X), ρ, d_e, τ, N_S
1: $N \leftarrow length\ (X)$;
2: $\widetilde{N} \leftarrow N - (d_e - 1)\tau$;
3: $d_w \leftarrow d_e\tau - 1$;
4: $\{Z_t\}_{t=1}^{\widetilde{N}} \leftarrow embed$ (E-SRE(X), d_e, τ);
5: $\mathcal{A} = \{z_t/\ t = 1, 2, ..., \widetilde{N}\}$;
6: **for** $k = 1 \rightarrow N_S$ **do**
7: **for** $j = 1 \rightarrow N - d_w$ **do**
8: $i \leftarrow 1$;
9: $s_1 \in \mathcal{A}$;
10: **while** $i < n$ **do**
11: $d_j = \|s_i - z_j\|$;
12: $\omega_j = e^{-\frac{d_j}{\rho}}$;
13: $p_j \leftarrow \omega_j / \sum_k \omega_k$;
14: $P(s_{i+1} = z_t) \propto p_j$;
15: $s_{i+1} = z_j$;
16: $i \leftarrow i + 1$;
17: **end while**
18: **end for**
19: $\{(s_t)_k\} \equiv \{(s_1)_k, (s_2)_k, ..., (s_N)_k\}$;
20: **end for**

The Algorithm requires: an E-SRE model of the circuit for the state variables X with/without thermal noise in some or all circuit components denoted by *E-SRE(X)*, the noise radius ρ, the embedding dimension d_e, the embedding lag τ, and the number of surrogates to be generated N_S. The algorithm begins with state space reconstruction of the circuit dynamics (line 4). It consists of representing the dynamical features of the circuit output E-SRE(X) in an alternative domain namely an Euclidian space $\mathbb{R}^{d_e}$ where d_e is the embedding dimension. By doing so, the points in $\mathbb{R}^{d_e}$ form an attractor $\mathcal{A}$ (line 5) that gives intuition about the circuit dynamics. Thereafter, embedding points of neighboring trajectories in the obtained attractor are used to create a new attractor with noisy trajectories (lines 10-17); The algorithm chooses an initial condition s_1 randomly from the reconstructed attractor $\mathcal{A}$ (line 9). For the following noisy attractor point, a near neighbor $z_j \in \mathcal{A}$ is then chosen with a probability commensurate to the noise radius ρ (line 14). The introduction of this dynamical noise by the surrogate generation algorithm will obliterate any deterministic dynamics of the circuit while preserving periodicity. Hence, chaotic circuit dynamics lead to distinct trends of their surrogates produced by this method.

B. Gaussian Kernel Test Statistic

The Gaussian Kernel (GK) test is a measure of correlation dimension d_c which is the dimensionality of the circuit attractor $\mathcal{A}$ [13]. It is mathematically defined by Equation (3). It uses the Gaussian kernel function (Equation (4)) that is more convenient for calculating the effect of Gaussian noise.

$$d_c = \lim_{h \to 0} \lim_{N \to 0+\infty} \frac{log\ \hat{T}_m(h)}{log\ h} \tag{3}$$

$$where\ \ \hat{T}_m = \frac{1}{N} \sum_i \sum_{j \neq i} \left(\frac{1}{N-1} e^{\frac{\|x_i - x_j\|^2}{4h^2}}\right) \tag{4}$$

where *h* denotes the bandwidth, and *N* denotes the number of estimation points. Our choice for this test is explained by the fact that it has been proven to provide a rigorous estimation of correlation dimension even for a noise level 50% higher than the ideal signal.

IV. Applications

In this section, we report the results of the application of our methodology on three AMS circuits. All computation and circuit models were performed in a MATLAB environment and were run on a 64-bit Windows 7 machine with 2.8 GHz processor and 24 GB memory. The type of hypothesis testing used is the one tailed test with the level of significance α=5%.

A. Colpitts Oscillator

A Colpitts oscillator is a combination of a transistor amplifier and an LC circuit as shown in Fig. 2.The Colpitts circuit behavior has been reported to exhibit chaotic behavior [14]. We model its behavior by the following E-SREs:

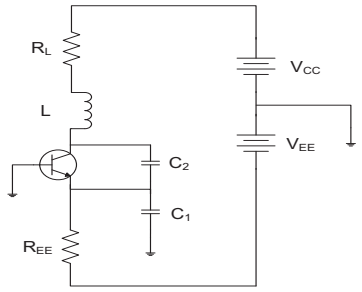

Fig. 2. Colpitts oscillator

$$\begin{aligned}
i_B(n) &= if(V_{BE} > V_{Th}, \frac{V_{BE}(n) - V_{Th}}{R_{ON}},\ 0) \\
i_c(n) &= if(true,\ \beta i_B(n),\ 0) \\
V_{CE}(n+1) &= if(true,\ V_{CE}(n) + \delta_t \frac{i_L(n) - i_c}{C_1},\ 0) \\
V_{BE}(n+1) &= if(true,\ V_{BE}(n) - \frac{\delta_t}{C_2} \\
&\quad (\frac{V_{EE} + V_{BE}(n)}{R_{EE}} + i_L + i_B)),\ 1) \\
i_L(n+1) &= if(true,\ i_L(n) + \delta_t(V_{CC} - V_{CE}(n) + \\
&\quad V_{BE}(n) - i_L(n)R_L),\ 0)
\end{aligned} \tag{5}$$

Table I summarizes the simulation and surrogate generation parameters for the Colpitts circuit. Fig. 3 illustrates both the original and reconstructed attractor of the Colpitts oscillator behavior using the embedding dimension (d_e, τ) given in Table I. The similarity of both attractors demonstrates the appropriate choice of embedding parameters.

TABLE I
SIMULATION PARAMETERS OF THE COLPITTS CIRCUIT

Parameter	Value	Parameter	Value
R_{EE}	0.904	R_L	35
C_1, C_2	54e-9	R_{EE}	400
R_{ON}	100	V_{CC}	5
V_{EE}	-5	V_{Th}	0.75
β	94	d_e	5
τ	3	ρ	0.003
N_S	100	N	3600

The importance of an adequate selection of the noise radius ρ is shown in Fig. 4. For instance, if ρ is too large ($\rho = 0.01$), the surrogate generation algorithm will introduce too much randomization and the surrogates will no longer resemble the circuit output z (see Fig. 4(c)). Conversely if ρ is too small ($\rho = 0.001$), the algorithm will introduce insufficient randomization, and surrogates will be identical to the output as shown in Fig. 4(b).

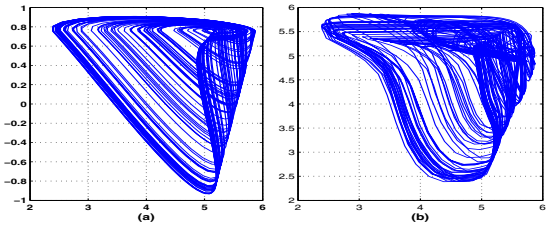

Fig. 3. Original attractor of Colpitts output (a), reconstructed attractor (b)

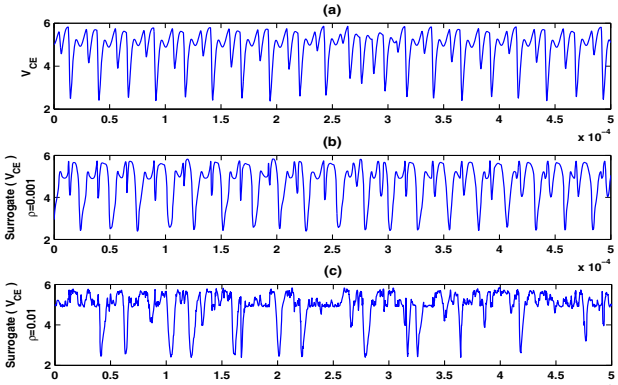

Fig. 4. The V_{CE} output and its surrogate for different noise radius ρ

Figure 5 depicts the GK correlation dimension d_c of the V_{CE} output (dashed line) and its corresponding 100 surrogates (dotted line). It can be observed that our approach successfully probes the chaotic behavior of the Colpitts circuit. For instance, the $d_c(V_{CE})$ is significantly different from those of the surrogates and so it falls in the rejection region (see Fig. 5). This leads to rejection of the noisy dynamics hypothesis and consequently proves the chaotic circuit dynamics.

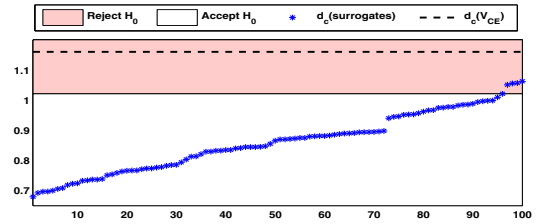

Fig. 5. Analysis results for chaotic Colpitts circuit

B. Third Order Σ-Δ Modulator

We consider the third order Σ-Δ modulator depicted in Fig. 6 and modeled as a system of E-SREs given by Equations (6).

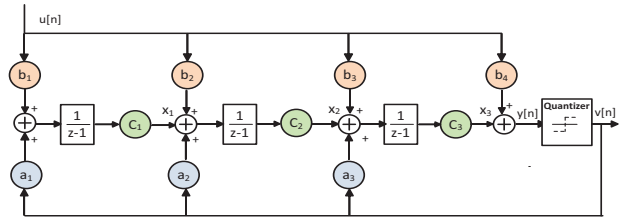

Fig. 6. Third Order Σ-Δ Modulator

$$
\begin{aligned}
v(k+1) &= if(P_{th}(k), -a, a) \\
x_1(k+1) &= if(P_{th}(k), x_1(k) + b_1u(k) - a_1a, \\
&\quad x_1(k) + b_1u(k) + a_1a) \qquad (6) \\
x_2(k+1) &= if(P_{th}(k), c_1x_1(k) + b_2u(k) + x_2(k) - \\
&\quad a_2a,\ c_1x_1(k) + x_2(k) + b_2u(k) + a_2a) \\
x_3(k+1) &= if(P_{th}(k), c_2x_2(k) + x_3(k) + b_3u(k) - \\
&\quad a_3a,\ c_2x_2(k) + x_3(k) + b_3u(k) + a_3a) \\
\text{where } P_{th}(k) &= c_3x_3(k) + u(k) \geq 0
\end{aligned}
$$

The following parameters of the circuit were computed using the Delta Sigma MATLAB Toolbox [15]:

$$a = 2,\ A = B = \begin{pmatrix} 0.044 \\ 0.2881 \\ 0.7997 \end{pmatrix},\ C = \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix}$$

In [8], the author proved that Σ-Δ modulators can reproduce chaos if it is fed by a chaotic input. This is a very important feature of Σ-Δ modulators in communication applications such as encryption and cryptography. Therefore, we will use our methodology to verify the Σ-Δ modulator given in Fig. 6, with the chaotic input fed from the Colpitts Oscillator studied in Section IV-A. Fig. 7 shows the time variation of the quantized output *V* for sinusoidal input (Fig. 7 (a)) and a chaotic input signal (Fig. 7(b)).

By using GK correlation dimension, we verify the circuit using the proposed methodology in the presence of thermal noise and chaos. Our results shown in Fig. 8(b) are in good agreement with the results in [8]. Indeed, the correlation dimension of the output *V* (dashed line) is very different from its corresponding surrogates (dotted line). This violates the hypothesis that the apparently random output is generated from

a noisy modulator. In contrast, in the presence of thermal noise Fig. 8(a), there was no apparent distinction between the two. Hence, H_0 holds and consequently the circuit exhibits noise.

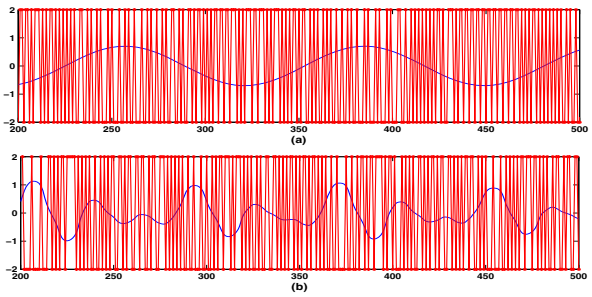

Fig. 7. Quantized sinusoidale wave (a) and chaotic (b) inputs

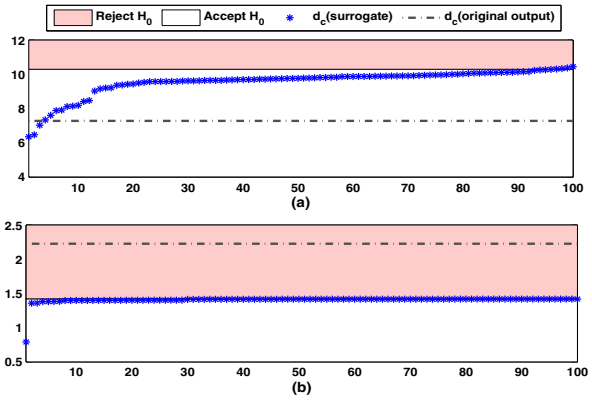

Fig. 8. Chaos verification for noisy modulator (a), and modulator fed with chaotic input (b)

C. Phase Locked Loop

PLLs are widely used circuits as modulators and demodulators in communication systems. In this section, we verify a third order PLL that serves as FM demodulator [16]. In this PLL, a multiplier Phase Detector (PD) and a resonant Low Pass Filter (LPF) are deployed as shown in Fig. 9.

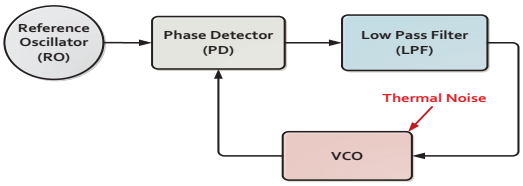

Fig. 9. Conventional PLL block diagram

The PLL dynamics are governed by the following E-SREs:

$$
\begin{aligned}
\varphi(n+1) &= if(true,\ \varphi(n) + \delta_t\ f_n,\ 0) \\
\Psi(n+1) &= if(true,\ \Psi(n) - \delta_t\ m\ f_n\ sin(\varphi(n)),\ \pi) \\
x(n+1) &= if(true,\ x(n) + \delta_t\ (\Omega_n - k_n\ z(n)),\ 0) \\
y(n+1) &= if(true,\ y(n) + \delta_t\ (\sin(x(n) - \Psi(n)) + \\
&\qquad (g-2)\ y(n) - \frac{g-1}{g}\ z(n)),\ 0) \\
z(n+1) &= if(true,\ z(n) + \delta_t\ (g\ y(n) - z(n)), 1)
\end{aligned}
\tag{7}
$$

where the state variables φ, Ψ, x, y, and z stand for modulating signal, frequency of modulation, phase difference between PLL input and VCO output, PD output, and LPF output, respectively. As the control parameter m changes, the dynamics of the PLL circuit change till culminating to chaotic regime. For instance, the circuit operates in periodic regime for $m = 0$ while chaotic dynamics occur for $m = 10$. Figure 10 depicts the time domain behavior of the PD output y for periodic (panel(a)), chaotic (panel(b)), and noisy behavior (panel(c)). It can be remarked that the chaotic output reveals a similar behavior to the noisy output simulated with thermal noise in the VCO. This demonstrates the need to assess the real source of random-like behavior observed in nonlinear AMS circuits during the design process. A phase diagram of the PLL attractor is depicted in Fig. 11.

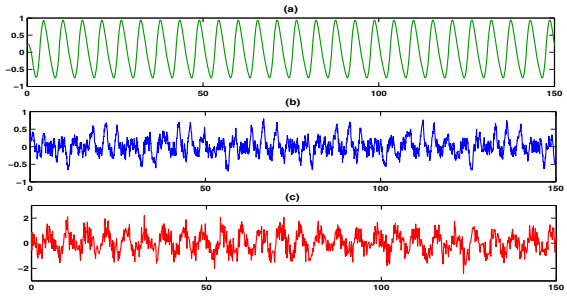

Fig. 10. Time variation of Y for periodic (a), chaotic (b), and noisy (c) regimes

TABLE II
SIMULATION PARAMETERS OF THE PLL CIRCUIT

Parameter	Value	Description
f_n	0.904	normalized frequency of the modulating signal
m	10	modulating index
Ω_n	1.2	normalized detuning
d_e	5	embedding dimension
k_n	0.6511	normalized loop gain
g	1.728	filter gain
τ	10	embedding lag
ρ	0.0170	noise radius
N_S	100	number of surrogates

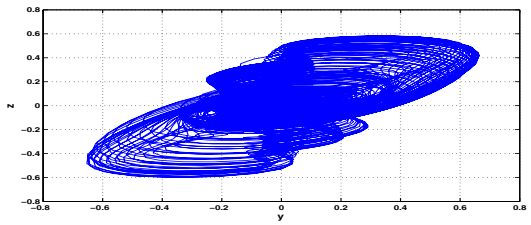

Fig. 11. Attractor of the PLL circuit during chaotic regime

The GK correlation dimension acquired from the the PLL circuit output y (dashed line) and 100 surrogates (dotted line) is shown in Fig. 12 for chaotic behavior (m=10) and in Fig. 13 for noisy behavior (m=0). A good qualitative agreement between the results of our methodology and the theory [16] is demonstrated; Indeed, the correlation dimension of the original output (dashed line) is very different from its corresponding surrogates (dotted line) in the chaotic case. This violates the hypothesis that the apparently random output is generated from a noisy circuit and hence indicates the deterministic dynamics

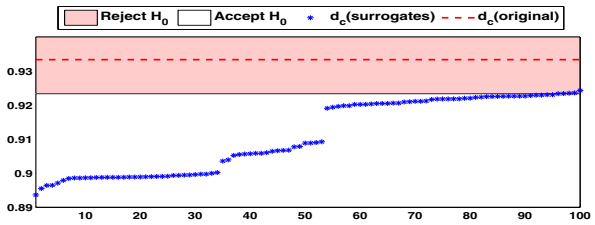

Fig. 12. Verification of PLL in chaotic regime

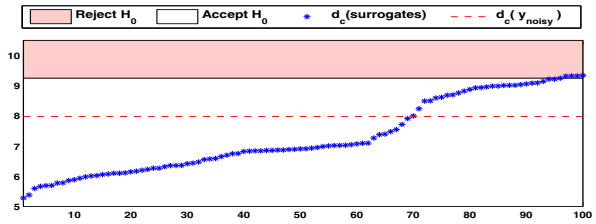

Fig. 13. Verification of PLL in Noisy regime

of the circuit. Consequently, the proposed methodology was able to successfully distinguish the noise like behavior exhibited by deterministic chaotic circuit from the stochastic noisy PLL.

D. Comparison with Lyapunov Exponent Method

In order to demonstrate the efficiency of the proposed methodology, the Lyapunov Exponent (LE) measure was carried out for the previously analyzed circuits under the same simulation conditions and for the same circuits outputs. The results of chaos verification and simulation time are recapitulated in Table III. The obtained results using our approach are in good agreement with those obtained with the LE technique for the Coplitts circuit and Σ-Δ Modulator. However, a failure to discriminate the noisy behavior of PLL has been detected (see Table III); Thermal noise in the VCO creates sensitivity to initial conditions of the PLL design that triggered the finding of a positive Lyapunov exponent which is a signature of chaos. In fact, a maximum exponent $\lambda = +0.0154$ has been obtained while the circuit exhibits thermal noise in the VCO and not chaotic behavior. Moreover, a simulation time acceleration is obtained using our methodology. Indeed, when adopting our approach, the simulation time was minimized from thousands of seconds to hundreds of seconds as shown in Table III.

TABLE III
ACCURACY AND SIMULATION TIME COMPARISON

	Colpitts Oscillator		3^{rd} order Σ-Δ Modulator		PLL	
	Our Method	LE	Our Method	LE	Our Method	LE
Simulation Time [Sec.]	164.7	709.7	196.3	985.4	247.3	1213.4
Chaos\Noise Detection	√	√	√	√	√	×

×: Failure in detecting circuit dynamics.
√: Successfully detecting circuit dynamics.

V. CONCLUSIONS

In this paper, a novel methodology to statistically assess chaos from noise in AMS circuits is proposed. The circuit is modeled using Extended System of Recurrence Equations. The verification approach is based on hypothesis testing and surrogate generation method to decide whether to reject or accept the hypothesis that the unpredictable circuit behavior emerges from noisy design. Our methodology has been successfully employed on a Colpitts oscillator, a third order Σ-Δ modulator and a third order PLL circuit. The main advantages of the proposed methodology are: (1) It improves robustness to thermal noise. For instance, our approach successfully discriminates noise in PLL while traditional techniques such as LE method fails to do so; (2) It sufficiently reduces the simulation time to around 5 times compared to the LE method; and (3) It is applicable to simulation traces when no mathematical model of the design is available. We believe that the proposed methodology will be a handy tool to give insight to designers about the onset of chaos in AMS circuits.

As future work, we plan to verify larger AMS circuits with other types of noise, such as $1/f$ noise and jitter. By doing so, we will be able to assess the limitations of the proposed methodology. Additionally, we aim to extend the proposed approach to discriminate simple chaos from hyperchaos.

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