Reliability Analysis of CMOS Rambus Oscillator under Device Mismatch Effects

Ibtissem Seghaier and Sofiène Tahar
Department of Electrical and Computer Engineering
Concordia University, Montreal, Quebec, Canada
Email:{seghaier, tahar}@ece.concordia.ca

***Abstract*—This paper introduces an approach that uses transient sensitivity analysis and state space verification to assess the reliability of Rambus oscillators due to device mismatch. The transient sensitivity analysis aims to truncate the high dimensional parameter variations space into a reduced subspace. Thereafter, a phase-space pattern matching verification approach is performed on this reduced subspace to estimate the yield rate using new measures called Recurrence Rate and Recurrence Periodicity Entropy. The proposed approach is illustrated on a four stage CMOS Rambus oscillator. The obtained results demonstrate a far faster yield assessment with a superior accuracy compared to Monte Carlo technique.**

I. Introduction

As Integrated Circuit (IC) technologies aggressively scaled to lower feature sizes and circuit applications moved to higher frequency bands, analog designers face new challenges in addition to a host of physical and functional constraints. Large scale process variability in modern circuits has become a major concern in the design of many analog circuits. In sharp contrast to the scaling down of modern device feature sizes, variability in the process parameters expand significantly exhibiting different device characteristics. In particular, device mismatch is pervasive and became a clear threat to analog circuits reliability [1] which culminates in yield loss.

Oscillators are one of the fundamental analog building blocks. They are commonly used in analog signal processing and electronics as clock generator, clock recovery, and integrated frequency synthesizer circuits [2]. They are designed to generate a periodic signal with small variations in amplitude and phase even in light of process variations and noise disturbances. The verification of these analog blocks is cumbersome and complicated by the continuing technology scaling. In particular, the challenge of verifying even stages differential ring oscillator (a.k.a. Rambus oscillator) is pinpointed by *Rambus* that now bears his name [3]. It is a real design issue faced in industry where oscillation failures were reported on several fabricated chips [4]. Different techniques have been proposed in the literature to verify the Rambus oscillator dynamics.

In [5], a method for locating DC-equilibrium points is proposed. Based on the stability analysis of each equilibrium point, the Rambus oscillator deemed to not drift in lock-up. However, this method suffers from two shortcomings: (1) It does not guarantee uniqueness of the stable oscillation behavior nor rule out the possibility of diminishing oscillation owing to unstable high order oscillatory modes (2) It does not consider the possibility of chaos onset in circuit behavior [6]. In [7], the authors proposed a pattern matching technique which ascertains the oscillation of Rambus by comparing its dynamics to the ideal one. The verification is conducted in the time domain and a new measure called Longest Closest SubSequence (LCSS) is used to account for process variation effects. Although promising results were reported using this technique, it has some limiting shortcomings for practical use. For instance, it requires the outputs of the circuits under verification to have the same length. Furthermore, it has quadratic complexity ($O(n^2)$) and does not automatically handle horizontal offset in the oscillator behavior.

The main focus of this paper is the reliability analysis of the Rambus oscillator due to device mismatch. More precisely, we are interested in assessing parametric yield for the Rambus oscillator. In order to address some of the shortcomings of the aforementioned approaches, we propose a novel method that uses sensitivity analysis and dynamical theory to verify the circuit. The verification is conducted not in the time nor frequency domains but alternatively in the phase space where we derive new clustering measures to detect non-oscillatory behaviors.

The rest of the paper is organized as follows: In Section II, we detail the proposed reliability analysis scheme of the Rambus oscillator circuits. Experimental results of the verification of a four stage CMOS Rambus oscillator in the presence of mismatch are reported in Section III. Section IV summarizes the contributions of this paper and provides future work hints.

II. Proposed Reliability Analysis Approach

Given a Rambus oscillator circuit model of the form $X = f(x, p, u)$, where x is a vector of state variables, f is a system of ordinary differential equations, p represents circuit parameters and u stands for initial condition uncertainties, we aim to verify the circuit robustness to device mismatch disturbance under all admissible values of u. The proposed approach is depicted in Figure 1. The Rambus oscillatory behavior is verified against a given specification. To do so, a number of N samples of the circuit parameters p, which is affected by mismatch, are generated from a Gaussian distribution according to the Pelgroms model. Then, we reduce the generated parameter (both electrical and geometrical) space variation due

978-1-5386-4859-9/18/$31.00 ©2018 IEEE

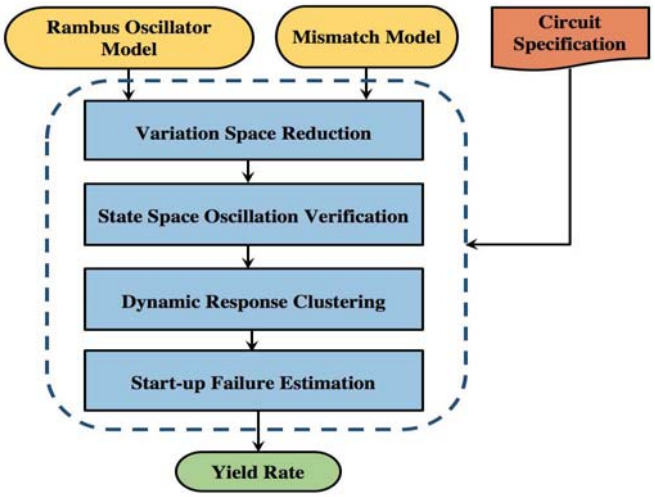

Fig. 1. Rambus oscillator verification

to mismatch to the actual influential parameters on the Rambus circuit oscillatory behavior. The variation space reduction is attained through a transient sensitivity analysis method. Next, we verify the lock-up/free oscillatory behavior in the state space using dynamical system theory [8]. Afterwards, start-up failures are estimated through a clustering procedure based on new verification measures inspired from DNA matching. The verification and clustering approaches are only conducted on the reduced parameter space variation which will significantly relieve the verification burden (i.e., time and memory usage) Finally, the parametric yield rate is assessed as follows:

$$Y_{parametric} = \frac{\text{Number of lock-up free Rambus circuits}}{\text{Total number of circuits under verification}} \quad (1)$$

A. Mismatch Model

Mismatch is an undesirable effect that arises in IC fabrication. It is a limiting factor of the accuracy and reliability of circuits, in particular oscillators. Due to mismatch, two nominally equal designed transistors display different absolute nominal parameters and consequently different electrical behaviors (i.e., operating points and other circuit characteristics differ from their intended values). In general, mismatch can be classified into: *systematic* and *random* as illustrated in Figure 2.

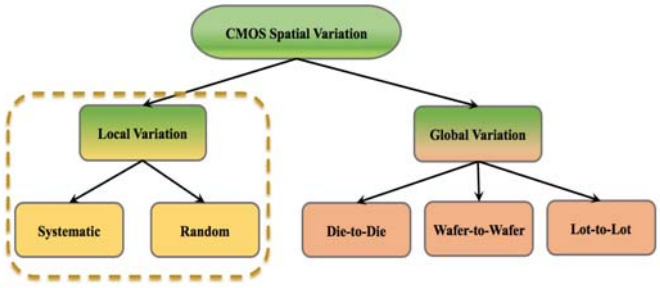

Fig. 2. CMOS spatial reliability issues

In this paper, we are interested in verifying random local mismatch impacts on Rambus oscillators. We employ the Pelgrom's simplified model [9] for local mismatch in MOS transistors to characterize the electrical circuit parameters variations, namely the current factor (β) and the threshold voltage (V_{th}) expressed by Equations (2) and (3), respectively.

$$(\frac{\sigma(\mathbf{\Delta}\beta)}{\beta})^{\mathbf{2}} = \frac{\kappa_{\beta}^{\mathbf{2}}}{\mathbf{WL}} \quad (2)$$

$$\sigma_{v_{\mathbf{th}}}^{\mathbf{2}} = \frac{\kappa_{v_{\mathbf{th}}}^{\mathbf{2}}}{\mathbf{WL}} \quad (3)$$

where κ_{β} and $\kappa_{v_{th}}$ are technology-dependent parameters, W and L refer to the width and the length of the transistors, respectively. For p-substrate, the PMOS transistor will have $\kappa_{v_{th}} \sim 1.5 \times \kappa_{v_{th}}$ NMOS.

B. Variation Space Reduction

This section presents the mismatch variation space reduction based upon the use of Fourier Amplitude Sensitivity Test (FAST) [10] on the Rambus oscillation property with respect to both electrical and physical parameters.

Definition II.1. *Sensitivity analysis is the study of how the variation in the circuit output of a behavioral oscillator model can be apportioned to different sources of variation in the circuit parameters and/or initial conditions. It introduces sensitivity indexes that reveal complicated high-order derivatives and coupling effects among circuit parameters.*

The FAST sensitivity concept is illustrated in Figure 3. Conversely to local sensitivity analysis which analyzes the local rate deviations of a circuit parameter, FAST considers variations of parameters in the whole variation space simultaneously, and therefore provides more reliable results. We are interested in measuring the sensitivity of the Rambus circuit oscillatory behavior to the uncertainty of the circuit parameters due to mismatch. More precisely, we are interestd in revealing non-influential parameters so they can be set to their nominal values and hence prune the variation space. To characterize these non-influential parameters, circuit parameters are ranked according to their contributions in the variance of the Rambus oscillation frequency as shown in Figure 3. The variance over the (*p-1*)-dimensional parameter space x_{-i}, consisting of all circuit parameters except p_i is defined as follows:

$$V_{x_{-i}}(y|x_i = x_i^*) \quad (4)$$

Because the true value of X_i is unknown, we average over all possible values of x_i:

$$E_{x_i}(V_{x_{-i}}(y|x_i)) \quad (5)$$

The smaller this quantity, the more important the contribution of x_i to the variance of the rambus circuit output y. Indeed, using the law of total variance, we get:

$$V(y) = V_{x_i}(E_{x_{-i}})(y|x_i) + E_{x_i}(V_{x_{-i}}(y|x_i)) \quad (6)$$

$$1 = \underbrace{\frac{V_{x_i}(E_{x_{-i}})(y|x_i)}{V(y)}}_{S_{i_F}} + \underbrace{\frac{E_{x_i}(V_{x_{-i}}(y|x_i))}{V(y)}}_{S_{i_T}} \quad (7)$$

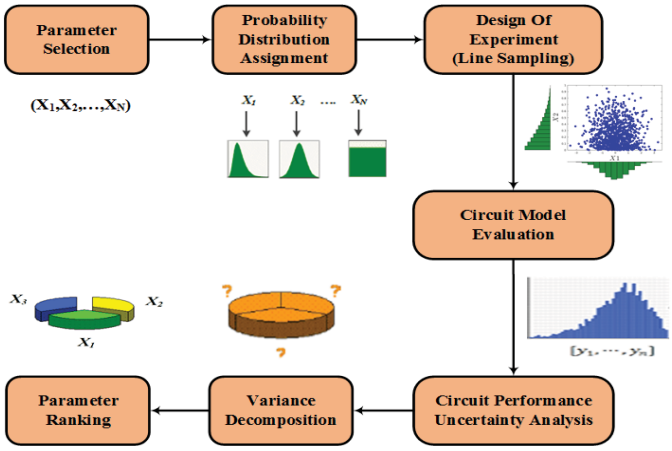

Fig. 3. FAST sensistivity analysis procedure

where S_{i_F}, S_{i_T} stand for the first order sensitivity index and total order sensitivity index for parameter x_i, respectively. From Equation (6), we conclude that first order sensitivity index verifies $S_i \leq 1$. Hence, it will be used as ranking index to characterize influential and non-influential mismatch parameters.

C. Dynamic Response Clustering

In this section, we define two new measures to cluster oscillatory and lock-up Rambus behavior. The first measure is the state space recurrence (RR) [11], which is defined as follows:

$$RR = \frac{1}{N-k} \sum_{j-i=k} CR(i,j) \tag{8}$$

$$\text{with } CR(i,j) = \Theta(x(t) \subset B(x(t+\delta t), \varepsilon) \tag{9}$$

where Θ is the Heaviside function, $B(x,\varepsilon)$ is a hypersphere of radius $\varepsilon > 0$ around the state variable x in the state space, and $x(t) \not\subset B(x(t+s),\varepsilon)$ for $0 < s < \delta t$, N is the length of the circuit output y.

The second measure is the Recurrence Periodicity Entropy (RPE) [12], which measures the average uncertainty in the periodicity density of the circuit output based upon the entropy. This measure, unlike the Fourier transform, does not require the assumptions of linearity, Gaussianity nor dynamical determinism.

$$H_{norm} = -(\ln T_{max})^{-1} \sum_{t=1}^{T_{max}} x(t) \ln x(t) \tag{10}$$

RPE is equal to 0 ($H_{norm} = 0$) for perfectly periodic oscillator and is equal to 1 ($H_{norm} = 1$) for purely stochastic oscillation (e.g., white noise). In theory, all RPE values lies in $0 \leq H_{norm} \leq 1$.

III. Experimental Results

Many different types of Rambus oscillators are presented in the literature. They mainly differ with respect to the number and the implementation of the inverter stages. In the sequel, we report the results of the application of our approach in a conventional realization of the CMOS Rambus oscillator. All computation and circuit models were performed in a MATLAB environment and were run on a 64-bit Windows 7 server with 2.8 GHz processor and 24 GB memory.

A. Four-Stage CMOS Rambus Oscillator

We consider a Rambus oscillator made with four stages of single-ended inverters chain as shown in Figure 4 that is defined as a verification challenge in [4]. Each stage has two forward inverters (labeled fwd) connected by a pair of cross-coupling inverters (labeled cc). Each inverter in its turn is composed of *N-channel* and *P-channel* transistors connected at their drains. The ODE model of the Rambus oscillator has

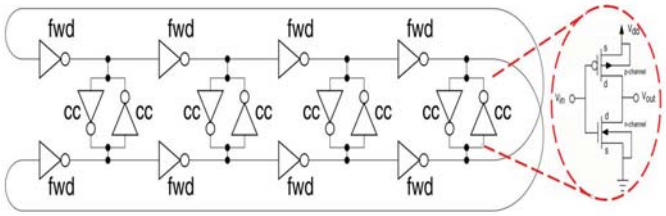

Fig. 4. Four stage Rambus oscillator schematic

eight state variables $(x_i)_{i=1}^{8}$ which are the voltage nodes in every inverter output on both the forward and cross-coupling paths. Hence, the circuit has an 8-dimensional state space. For illustration purposes, we limit the visualization to three state variables in the $(x_1 \times x_4 \times x_8)$ space. The attractor in the cases of free oscillation and lock-up are shown in Figures 5(a) and 5(b), respectively, It can be remarked that the trajectories of the circuit behavior in the case of free oscillation (Figure 5(a)) settles to a periodic attractor. It follows that the start-up property is guaranteed in this case and a stable oscillation will eventually settle. Conversely, in the case of lock-up the Rambus circuit trajectory diverges. It is known that size ratio is the most influential parameter on the circuit oscillation. In order to better assess the influence of the different parameters of the transistor size ratio (r) on the oscillation failure, we conducted the sensitivity analysis of the Rambus circuit to oscillation property for different transistors widths (W_{ni}, W_{pi}) and lengths (L_{ni}, L_{pi}) on both the forward (fwd) and cross-coupling (cc) inverters. Results demonstrate that the size of

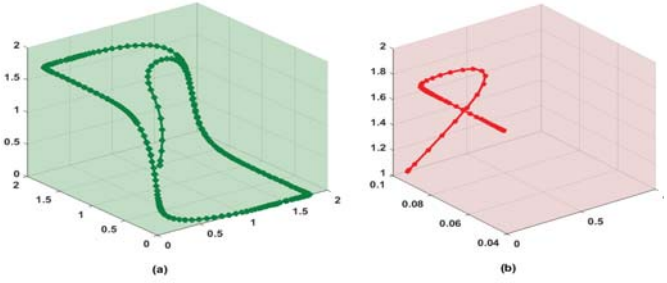

Fig. 5. State Space Rambus circuit responses

TABLE I
YIELD ESTIMATION RESULTS FOR THE FOUR STAGE CMOS RAMBUS OSCILLATOR

		W_n(cc)	W_p(cc)	W_n(fwd)	W_p(fwd)
MC	Runtime (h)	7.38	7.44	7.42	7.39
	Yield (%)	75.8	72.6	79.2	76.8
Our approach	Runtime (h)	3.54	3.49	3.38	3.37
	Yield(%)	73.7	71.9	78.9	75.5

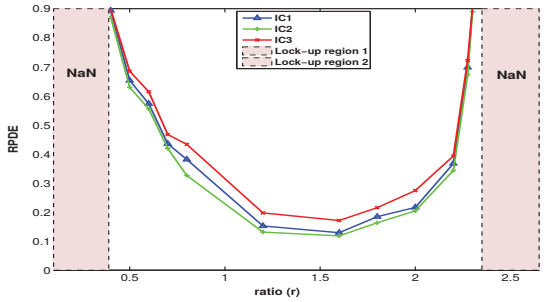

Fig. 6. Variation of the Recurrence Periodicity Entropy for different transistor size ratio

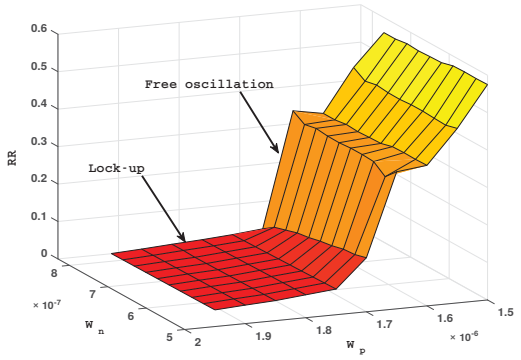

Fig. 7. Recurrence rate variation with transistors (cc) widths variations

the (cc) inverters more particularly the transistors widths has more influence on the Rambus circuit oscillation property. The variation of RPE for different transistor size ratio (r= $\frac{size(cc\ inverter)}{size(fwd\ inverter)}$) and different initial conditions are depicted in Figure 6 wherein the lock-up behavior is marked by a NaN Matlab value ($ln(\infty)^{-1} \times \infty = NaN$). Figure 7 depicts the variation of RR computed using our dynamic response clustering scheme with mismatch in the N-mos and P-mos transistors widths in the (cc) inverters. The results confirm the finding of the FAST sensitivity analysis. In fact, W_p affects more the oscillation of the Rambus circuit. It can be noticed that by increasing the P-mos width, the circuit presents two regions: 1- a non-oscillation (lock-up) region for $W_p \geq 1.7\mu m$ that is marked by a zero recurrence rate (see Figure 7); and 2- an oscillation-free region for $W_p < 1.7\mu m$ that has a non-zero increasing recurrence rate. We compare the yield rates obtained using our method with standard Monte Carlo (MC) technique. As depicted in Table I, our proposed reliability analysis approach achieves a significant speedup compared to Monte Carlo (MC) method. This is because our verification scheme is conducted in the abstracted state space domain while MC works on the time domain and hence requires more verification time. Moreover, our technique is able to achieve higher failure probability rate (i.e., lower yield rate) by detecting start-up failures that were uncovered by the MC method.

IV. CONCLUSION

This paper describes an approach based on state space verification to account for mismatch in Rambus oscillator circuits. A transient sensitivity analysis method is used to prune the parameter variation space. The effect of mismatch is then studied by performing state space analysis and dynamic response clustering to detect start-up failures in terms of yield rate. The efficiency of our approach is illustrated on a four-stage CMOS Rambus for 90nm technology process. A comparison with the standard time domain Monte Carlo analysis technique shows the advantages of our method in terms of yield accuracy and runtime. Our future plan is to show the effectiveness of our method on larger Rambus oscillator architectures and to develop a method that could handle catastrophic yield analysis.

REFERENCES

[1] E. Maricau and G. Gielen, "CMOS reliability overview," *Analog IC Reliability in Nanometer CMOS*, pp. 15–35, 2013.

[2] J. Van Der Tang, D. Kasperkovitz, and A. H. Van Roermund, *High-frequency oscillator design for integrated transceivers*. Springer Science & Business Media, 2003, vol. 748.

[3] M. R. Greenstreet, "Verifying VLSI circuits," in *International Symposium on Automated Technology for Verification and Analysis*, 2009, pp. 1–20.

[4] K. D. Jones, J. Kim, and V. Konrad, "Some "real world" problems in the analog and mixed signal domains," *Designing Correct Circuits*, pp. 51–68, 2008.

[5] M. R. Greenstreet and S. Yang, "Verifying start-up conditions for a ring oscillator," in *ACM Great Lakes symposium on VLSI*, 2008, pp. 201–206.

[6] I. Seghaier, M. H. Zaki, and S. Tahar, "A statistical approach to probe chaos from noise in analog and mixed signal designs," in *IEEE Computer Society Annual Symposium on VLSI*, 2015, pp. 237–242.

[7] R. Narayanan, A. Daghar, M. Zaki, and S. Tahar, "Using LCSS algorithm for circuit level verification of analog designs," in *IEEE International New Circuits and Systems Conference*, 2012, pp. 185–188.

[8] A. Katok and B. Hasselblatt, *Introduction to the modern theory of dynamical systems*. Cambridge University Press, 1997.

[9] M. J. Pelgrom, A. C. Duinmaijer, and A. P. Welbers, "Matching properties of MOS transistors," *IEEE Journal of solid-state circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[10] A. Saltelli and R. Bolado, "An alternative way to compute fourier amplitude sensitivity test (FAST)," *Computational Statistics & Data Analysis Journal*, vol. 26, no. 4, pp. 445–460, 1998.

[11] I. Seghaier, M. H. Zaki, and S. Tahar, "Cross recurrence verification technique for process variation-resilient analog circuits," in *IEEE International Symposium on Circuits and Systems*, 2016, pp. 1294–1297.

[12] C. L. Webber Jr and N. Marwan, "Recurrence quantification analysis," *Theory and Best Practices*, 2015.