# Mating Sensitivity Analysis and Statistical Verification for Efficient Yield Estimation

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Abstract—Parametric yield is a significant threat to the reliability of nanoscale analog and mixed-signal circuits. A critical yet challenging problem of yield estimation is to account for multiple circuit performance. In this paper, we propose a novel nonparametric statistical verification methodology to efficiently estimate the parametric yield due to 65-nm technology for multiperformance constraints. Our proposed approach exploits the fact that circuit parameters variation has different impacts on the circuit performance. Hence, a global sensitivity analysis classifies the circuit parameters according to their influence on the desired circuit performances. Based on this classification, an efficient joint recurrence verification (JRV) algorithm, a procedure inspired from DNA analysis, is performed on the most "critical/influential" parameters. A global hypothesis testing procedure is then performed based on the computed JRV metrics. We demonstrate the effectiveness of our methodology on two benchmark circuits. The acquired results show the ability of our approach to handle multiple corners and multiple performances yield problems with up to 11× speedup compared to conventional techniques with an average error smaller than 3%.

*Index Terms*—Analog and mixed-signal (AMS) circuits, multiple performance, process variation, yield.

#### I. INTRODUCTION

LONG with the tremendous area, speed, and cost rewards A of today's technology scaling comes significant challenges in the design and verification of integrated circuits. In particular, the increased inevitable process-induced variability has become a major concern that substantially affects device parameters, such as channel length (L), gate width (W), threshold voltage  $(V_{\text{th}})$ , and oxide thickness  $(T_{\text{ox}})$ . Process variation may lead to large deviations in the circuit parameter values that can be great enough to violate the desired circuit performance [1]. This culminates in yield losses and extremely expensive design costs since circuits that do not meet the performance target are discarded. It is hence very crucial to develop an efficient and accurate verification framework to provide parametric yield (i.e., probability to meet the desired performance/specification in light of process variation) prediction early in the VLSI design flow [2]. This yield estimation framework is a foundation for circuit sizing [3], optimization [4], and performance enhancements [5].

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Monte Carlo (MC) is the mainstay standard parametric yield estimation approach for analog and mixed-signal (AMS) designs [6]. This approach can be elucidated in the following steps: 1) generating a set of random samples drawn from the process parameters models; 2) performing repeated simulation of the drawn samples and evaluating the circuit performance at all sets of these samples; and 3) estimating the parametric yield as the ratio of the samples that comply with the desired specification over the total number of simulation runs. Although, MC is easy to implement, its relative cost is far from small. It has slow convergence rate and its accuracy is directly tied to the number of simulation runs performed. To alleviate the inefficiency of the primitive MC approach, several speed enhancement techniques based on design of experiment have been proposed in the last decade. Existing MC variants, include Latin hypercube sampling (LHS) [7], importance sampling [8], and quasi-MC (QMC) methods [9]. However, most of these approaches are either circuit specific or perform poorly in high-dimensional parameter design space [10]. Moreover, all process variation parameters may not be at their worst levels during the same simulation run [11]. Given the above-mentioned limitations, a particular attention should be made to the selection of the samples drawn from the process parameter space rather than the blind conventional sampling. This way, a significant speed up can be attained by focusing on the most influential parameters on the desired circuit performance while guaranteeing a better verification coverage. "How to appropriately select the necessary, sufficient and most influential circuit parameters from the circuit process variation parameters?" is the question that has to be answered.

On the other hand, commonly used worst case tolerance analysis [12] technique, while computationally feasible, is not able to provide meaningful statistical data that can be deployed in yield estimation. Alternatively, response surface modeling (RSM) are promising alternative techniques to predict the yield [13] via circuit performance approximation as an analytical function of process parameters (e.g., W, L, and  $V_{\rm th}$ ). Although RSM techniques improve simulation efficiency, this is not without downfalls. Indeed, they have strict restrictive assumptions of linearity and normality. This fueled the need for a generic/nonparametric yield estimation scheme that retains the nonlinear and strongly nonlinear AMS circuits behavior while being model independent (i.e., distribution-free). Most of the aforementioned parametric yield prediction techniques are greedy sole performance estimation approaches. Multiple performances estimation is thereby handled through performing several independent single parametric yields. Nevertheless, this might significantly compromise the accuracy especially in the case of correlated circuit

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performances whose failure regions overlap. To alleviate the multiperformance correlation problem in yield estimation, there is an urgent need to incorporate multiple performance metrics simultaneously not only in the same performance domain but also in the same verification procedure.

In this paper, we present a novel methodology for fast and efficient yield estimation of AMS designs under multiple performance constraints. In the proposed methodology, we first introduce a global sensitivity analysis (SA) scheme, which is particularly acute for pinpointing the most critical circuit parameters in terms of variability on the desired circuit performances. The proposed SA scheme will serve as a guideline in defining the process parameters focus on the verification plan in order to smartly guide the verification stage through an effective sampling/good coverage of the process parameters space. Moreover, the proposed SA technique will help in identifying the noninfluential parameters on the yield loss so they will be fixed to nominal values. Second, a procedure called joint recurrence verification (JRV) that is inspired from pattern matching in DNA sequences is introduced to verify whether an analog circuit still satisfies its specification in light of process variation. The proposed verification approach is conducted in the state-space domain. This will permit multiple performances evaluations at the same time by projecting them into a multidimensional domain. To the best of our knowledge, this is the first work for reliable vield estimation that is able to handle multiple performances verification in the state domain with a guarantee of exhaustive verification coverage. We illustrate our methodology on two benchmark circuits. The first application involves a ring oscillator that we used as a proof of concept. The second application is a phase-locked loop (PLL) circuit.

This paper is organized as follows. Section II reviews existing AMS circuits parametric yield estimation techniques. Section III presents the research background. Section IV details the different steps in our multiperformance yield prediction methodology. Section V reports and discusses our experimental results. Section VI states our main conclusions.

## II. RELATED WORK

Yield analysis and estimation for AMS designs have been greatly debated and have become an appealing area of research in recent years [15], [16]. We review hitherto existing techniques for parametric yield analysis.

State-of-the-art parametric yield estimation techniques for AMS designs can be roughly divided into two categories: 1) parameter domain and 2) performance domain techniques. While parameter domain techniques are based on the characterization of a yield boundary defined by the design specification, performance domain techniques rely upon MC simulations.

Parameter Domain Techniques: These methods try to extract an analytical relation between the underlying process parameters and the circuit performances. RSM has been adopted to approximate the performances of interest as polynomial functions of process parameters in order to substitute expensive SPICE simulations. Most of the existing RSM techniques rely on linear approximations. This would sacrifice accuracy for speedup particularly in large scaled process variations where AMS circuit performances are strongly nonlinear. As demonstrated in [13], the resulting accuracy might be unacceptable with an absolute error of 9%. Thus, a quadratic RSM has been used [16] but at the cost of a much more difficult yield analysis. Other existing methods rely on a surface boundary, which is the separation between success and failure regions in the yield prediction. The yield is so estimated using a local search [17] or global search [2] by computing the volume of these failure regions without the need for circuit simulation. Nevertheless, such methods suffer from scalability issues with no more than three process parameters.

Performance Domain Techniques: MC [18] is the most widespread performance domain yield estimation technique thanks to its simplicity and general applicability. However, an MC analysis of large-sized circuits is highly inefficient and time consuming. Several speed-up techniques have been proposed to improve the primitive MC time efficiency and applicability. QMC [9], a variance reduction technique in which low discrepancy sequences (LDSs) are utilized to generate more homogeneously distributed process parameters samples rather than purely random ones. Hence, QMC techniques are able to provide better integration errors compared to primitive MC. Yet, QMC has a limited performance improvement with a convergence rate that is asymptotically superior to MC only for circuits with a moderate number of process parameters [7]. Although speedup enhanced QMC techniques using Latin supercube sampling have been proposed in [19] and [20], more efficient non-MC methods are needed.

#### III. PRELIMINARIES

## A. Sobol-Hoeffding Decomposition

Considering process variation and noise, the circuit dynamics can be lumped in the form of a system of stochastic recurrence equations (SSREs) (see section) given in (1) for  $t \in [0, T] \doteq \tau$  at time s

$$\bar{X}_{s+\Delta s}(\omega) = \bar{X}_{s}(\omega) + C(\bar{X}_{s}; P)\Delta s + \sigma(\bar{X}_{s}; P)(W_{s+\Delta s}(\omega) - W_{s}(\omega))$$
(1)

where  $\bar{X}_s$  is the set of circuit state variables,  $\Delta s$  is the time discretization step, W is a Wiener process which reflects the randomness in the circuit behavior introduced by noise disturbance, C is the drift function, and  $\sigma$  is the diffusion coefficient [21]. The process variation effect is represented as a random parameter P with known probability law (extracted from the technology library) in (1). The circuit behavior can be seen as a function of  $\omega$  and  $P: X_{s+\Delta s} = X(s, \omega, P)$ . Thus, we want to investigate the respective impact of the noise uncertainty  $\omega(t)$  and the parameters uncertainties P on the circuit performances. In the sequel, we recall the Sobol–Hoeffding decomposition (SHD).

Definition 1 (L<sub>2</sub> Functions):  $L_2(\mathcal{U}^d)$  is the space of realvalued squared integrable functions over the *d*-dimensional hypercube  $\mathcal{U}$ 

$$X : p \in \mathcal{U}^d \to X(p) \in \mathbb{R}$$
$$X \in L_2(\mathcal{U}^d) \Leftrightarrow \int_{\mathcal{U}^d} X(p)^2 dp < \infty.$$
(2)

 $L_2(\mathcal{U}^d)$  is equipped with the inner product  $\langle ., . \rangle$ 

$$\forall X, Y \in L_2\left(\mathcal{U}^d\right)$$

$$\langle u, v \rangle \coloneqq \int_{\mathcal{U}^d} X(p) Y(p) \ dp.$$
 (3)

The weighted space  $L_2(A, \rho)$  is an extension of  $L_2$  where

$$P \in \mathcal{A} = A_1 \times A_2 \times \dots \times A_d \subseteq \mathbb{R}^d$$
$$\rho : P \in \mathcal{A} \to \rho(P) \ge 0$$
$$\rho(P) = \rho_1(p_1) \times \dots \times \rho_d(p_d)$$

where  $\rho$  denotes the probability density function of the circuit parameters random vector *P* with mutually independent components.

Theorem 1: Any  $X \in L_2(A, \rho)$  (see Definition 1) admits a unique hierarchical orthogonal decomposition. Let  $P = (p_1, \ldots, p_d)$  in  $\mathbb{R}^d$ , the decomposition consists in writing the X(P) as the sum of increasing dimension functions [22]. The expansion in (5) exists and is unique under one of the following orthogonality conditions:

$$\int X_u(p_u)d\rho_{P_i} = 0 \ \forall i \in u, u \subseteq \{1, \dots, d\}$$
  
or  
$$\int X_u(p_u)X_v(p_v)d\rho_P = \langle X_u, X_v \rangle = 0 \ \forall u$$
$$v \subseteq \{1, \dots, d\}u \neq v.$$

The independence of the inputs and the orthogonality property in (5) ensures the global variance decomposition of the output X(P) as follows:

$$\mathbb{V}[X(P)] = \mathbb{E}\left[\left(X(P) - X_0\right)^2\right]$$
$$= \mathbb{E}\left[\left(\sum_{\{i_1,\dots,i_d\}\subset\{1,\dots,M\}} X_{i_1,\dots,i_d} \left(Pi_1,\dots,P_{i_d}\right)^2\right]\right]$$
$$= \sum_{\{i_1,\dots,i_d\}\subset\{1,\dots,M\}} \mathbb{E}\left[\left(X_{i_1,\dots,i_d}^2 \left(Pi_1,\dots,P_{i_d}\right)\right]\right]$$
$$= \sum_{i\neq\emptyset,i\subseteq\mathcal{D}} \mathbb{V}[X_i], \ \mathbb{V}[X_i] = \langle X_i, X_i \rangle.$$

 $\mathbb{V}[X_i]$  is interpreted as the contribution to the total variance  $\mathbb{V}[X(P)]$  of the interaction between parameters  $p_{i \in \mathcal{D}}$ . Hence, the Sobol–Hoeffding variance decomposition provides a very useful and rich means of analyzing the respective contributions of individual or set of parameters to the circuit output variability. For instance, it partitions the output variance amongst the uncertain factors of the circuit model. Given the structure of the circuit model described in (1), the hierarchical orthogonal SHD [22] of X gives

$$X(\omega, P) = X + X_{\omega}(\omega) + X_{P}(P) + X_{\omega,P}(\omega, P), \forall t \in \tau$$
$$\mathbb{V}[X] = \mathbb{V}[X_{\omega}] + \mathbb{V}[X_{P}] + \mathbb{V}[X_{\omega,P}].$$

Therefore, it is possible to determine the global SA as sensitivity measures (see Fig. 1) that define the fraction of variance due to individual effects as well as their interactions: noise only  $S_{\omega}$ , process variation only  $S_P$ , and the combined variation of noise and process variation  $S_{\omega,P}$ 

$$S_{\omega} = \frac{\mathbb{V}[X_{\omega}]}{\mathbb{V}[X]}, \quad S_{P} = \frac{\mathbb{V}[X_{P}]}{\mathbb{V}[X]}, \quad S_{\omega,P} = \frac{\mathbb{V}[X_{\omega,P}]}{\mathbb{V}[X]} \quad (4)$$
$$X(P) = X(p_{1}, \dots, p_{d}) = X_{0} + \sum_{i=1}^{d} X_{i}(p_{i})$$



Fig. 1. Global SA illustration.

$$+\sum_{i=1}^{d}\sum_{j=i+1}^{d}X_{i,j}(p_{i}, p_{j}) + \sum_{i=1}^{d}\sum_{j=i+1}^{d}\sum_{k=j+1}^{d}X_{i,j,k}(p_{i}, p_{j}, p_{k}) + \dots + X_{1,\dots,d}(p_{1},\dots, p_{d}).$$
(5)

## B. Multiple Parametric Yield Estimation

Given a circuit topology, the parametric circuit performance of interest g (e.g., the gain of an amplifier or the oscillation frequency of an oscillator) are functions of the circuit responses. The performance constraints can be expressed in the following standard form:

$$g_i(R(p)) \le 0 \ i = 1, 2, \dots, m$$
 (6)

where  $p \in \mathbb{R}^n$  stands for the circuit parameters,  $R : \mathbb{R}^n \to \mathbb{R}^m$ is the circuit response vector, m is the total number of performance constraints, and  $g_i$  is the *i*th performance metric. Any performance constraints can be reformulated in the standard form given in (6). For instance,  $g_i(R(p)) \leq C$ ,  $g_i(R(p)) \ge C$ , and  $g_i(R(p)) \in [C_{\min}, C_{\max}]$  can be expressed as:  $g_i(R(p)) - C \le 0, C - g_i(R(p)) \ge 0$ , and  $(g_i(R(p)) - C_{\min} \le 0)$ 0 &  $C_{\max} - g_i(R(p)) \ge 0$ , respectively. Given the performance constraints in (6), each element of  $g_i$  has a certain tolerated lower and/or upper bound. Hence, in the parameter space, a certain part of the performance distribution will be cut off wherein a part of the circuit parameter variation falls out of the acceptance region bordered by the specification limits set by the designers. From (6), the fraction of the distributions which are within the performance specification is called acceptance region  $A_p$  and it is mathematically defined as:  $A_p = \{p | g_i(R(p)) \le 0, \quad i = 1, 2, ..., m\}.$ 

Parametric yield is the percentage of circuits that satisfy the performance specification considering statistical parameter variations. In other words, it is the probability of satisfying the parametric requirements, i.e., the parameters p\* lead to acceptable performance and so belong to the acceptability region  $A_p$ 

$$Y(x) = P\{p \in A_p\} = \int_{\mathbb{R}^n} \phi_p(p) f_p(p, x) dp = E_p\{\phi_p(p)\}$$
(7)

where  $P\{.\}, \phi_p(p)$ , and  $E_p\{.\}$  denote the probability, an indicator function, and the expectation with respect to the random

variable p, respectively. The indicator function  $\phi$  is determined by the performance specification and its corresponding acceptance function described as

$$\phi(p) = \begin{cases} 1 \text{ (Pass) if } p \in A_p \\ 0 \text{ (Fail) otherwise.} \end{cases}$$

The *n*-dimensional integration in (7) has a canonical form and can be numerically approximated to:  $Y_{MC} = (1/N) \sum_{k=1}^{N} \phi_{\xi}(\xi)$  where  $Y_{MC}$  stands for MC-based yield estimator,  $\xi$  are independently drawn random samples from the parameter uncertainty domain, and *N* is the MC sample size. The yield estimation formulated in (7) is for a single performance metric. A generalization of the yield expansion in the case of multiple performances is defined as follows:

Yield = 
$$P\left(p \in \left(\bigcup_{i=1}^{m} A_{p}^{i}\right)\right)$$
. (8)

By applying the inclusion–exclusion principle [23] to (8), the total yield for m performance merits is expressed as

$$Yield = \sum_{i=1}^{m} P\left(p \in A_{p}^{i}\right) - P_{\text{overlap}}$$

$$P_{\text{overlap}} = -\sum_{i < j} P\left(A_{p}^{i} \cup A_{p}^{j}\right) + \sum_{i < j < l} P\left(A_{p}^{i} \cup A_{p}^{j} \cup A_{p}^{l}\right)$$

$$- \dots + (-1)^{m-1} P\left(p \in \left(\bigcap_{i=1}^{m} A_{p}^{i}\right)\right). \tag{9}$$

## IV. PROPOSED METHODOLOGY

The main objective of this paper is to assesses multiperformances circuit reliability in terms of parametric yield. An overview of the proposed methodology is depicted in Fig. 2. The process variation effects are captured within an SSRE. In order to optimize the verification step, a dimension reduction technique of the process parameter space is proposed. The proposed technique sorts the process parameters by influence weight and prunes the unimportant parameters. Then, the verification is performed on the state space domain of the circuit transient dynamics based on a statistical runtime verification approach. It mainly consists of the following main phases.

After modeling the circuit as an SSRE (i.e., behavior model that captures the stochastic behavior of the circuit), the first phase runs a transient global SA routine. It aims to quantify the impact of process variability on circuit performances as well as to identify critical circuit parameters variation driving the circuit failure. The aim of the SA is two folds: 1) improve the predictive capability of the next phase (i.e., yield estimation scheme) in terms of accuracy and tractability and 2) reduce the computational cost through screening out noninfluential parameters by setting their values to nominal values.

The second phase is the statistical yield estimation scheme. The circuit SSRE model is simulated for the circuit process parameters computed in the transient SA step. The circuit performance verification is then performed through a JRV scheme. A novel verification metrics are developed to score how close is the circuit behavior to the ideal one. Basically, three metrics are defined, namely recurrence rate (RR), maximum joint sequence ( $L_{max}$ ), and the recurrence periodicity (RP). The verification is conducted in



Fig. 2. Proposed parametric yield estimation approach.

the state space domain which allows simultaneous multiple performance/outputs verification. The yield rate is thereafter estimated based on a global hypothesis testing procedure on the derived JRV metrics.

## A. System of Stochastic Recurrence Equations

An SSREs [24] is a formalism that allows modeling uncertainties in AMS circuits in a unified analog/digital description. It is an extension to the ordinary differential equation, extracted from the well-known modified nodal analysis, with stochastic term that could model uncertainties such as noise disturbance. In the following, we briefly present the SSRE theory. An SSRE is a set of system recurrence equations with stochastic processes. Let us consider the following Itô process  $\{X_t, 0 \le t \le T\}$  stochastic differential equation (SDE) for a 1-D process with a 1-D driving Brownian motion

$$dX_t(\omega) = C(X_t, (\omega))dt + \sigma(X_t(\omega))dW_t(\omega)$$
(10)

where the stochastic variable  $W_t$  is a Brownian motion [25] (see Definition 2), the initial condition  $(X_{t_0} = X_0)$  and the diffusion coefficient  $\sigma$  are deterministic variables.

Definition 2 (Brownian Motion): A scalar standard Brownian process, or standard Wiener process over [0, T] is a random variable  $W_t$  that depends continuously on  $t \in [0, T]$ and satisfies the following conditions.

Condition 1: W(0) = 0 with probability 1.

Condition 2: For  $0 \le s < t \le T$  the random variable given by the increment  $W_t - W_s$  is normally distributed with mean zero and variance (t - s)  $(W_t - W_s \sim \sqrt{t - s}\mathcal{N}(0, 1))$ .

Condition 3: For  $0 \le s < t < u < v \le T$  the increments  $W_t - W_s$  and  $W_v - W_u$  are independent.

By integrating (10) between s and  $s + \Delta s$ , we will have

$$dX_{s+\Delta s}(\omega) = X_s(\omega) + \int_s^{s+\Delta s} f(X_{s+\Delta s}(\omega))dt + \int_s^{s+\Delta s} f\sigma(X_{s+\Delta s}(\omega))dW_{s+\Delta s}(\omega).$$
 (11)

Algorithm 1 Process Parameters Screening Flow **Require:**  $P(d), G(m), l, LB, UB, N^*$ 1: Compute the step size  $\Delta : \Delta = \frac{l}{2(l-1)}$ 2: Compute starting process parameter vector  $p^* = LB$ 3: for  $s = 1 \rightarrow d$  do for all  $g_k \in G$  do 4: 5: repeat Calculate the sampling matrix *C* as follows: 6:  $C = J_{(d+1,1)}LB + A_s(D(UB - LB))$  with  $A_s =$  $J_{(d+1,d)}p^* + \frac{\Delta}{2}[(2A - J_{(d+1,d)})D^* + J_{d+1,d}]Pr^*$ Compute Elementary Effects: the 7:  $E_{(s,k)} = \frac{g_k(C_i) - g_i(C_j)}{4}$ until  $r = N^*$ 8:  $\begin{aligned} & \mu_k^* = \frac{1}{N^*} \sum_{r=1}^{N^*} |E_{(s,k)}| \\ & \sigma_k^2 = \frac{1}{N^*} \sum_{r=1}^{N^*} E_{(s,k)} \\ & \mu = \frac{1}{N^*} \sum_{r=1}^{N^*} E_{(s,k)} \end{aligned}$ 9: where 10: end for 11:  $GI_s = \max_{k=1}^{m} \left( \sqrt{\mu_k^2 + \sigma_k^2} \right)$ 12: k = 1, ..., m $[P^n, P^i]$  = Assess parameter influence  $(GI_s)$ 13: 14: end for 15: return  $P^n$ ,  $P^i$ 

The Euler scheme [26] consists in approximating the SDE as follows:

$$\bar{X}_{s+\Delta s}(\omega) = \bar{X}_{s}(\omega) + f(\bar{X}_{s}(\omega))\Delta s + \sigma(W_{s+\Delta s}(\omega) - W_{s}(\omega)).$$
(12)

*Example:* Consider a simple series RL circuit with white noise at the input voltage source  $V_{in}$ , the SSRE describing its behavior is as follows:

$$I_{s+\Delta_s} = I_s + \frac{\Delta_s}{L} (V_{\text{in}_s} + \sigma_{\text{noise}} (W_{s+\Delta s}^n - W_s^n) - RI_s).$$
(13)

## B. Transient Sensitivity Analysis

When dealing with the problem of large process variation spaces, a natural verification strategy is to first reduce the parameter variation space by some selection (screening or filtering) process, and then to verify the circuit properties on the reduced process parameters set. The main objectives at this step are twofold: 1) how to identify the critical parameters or the group of circuit parameters related to the variation in circuit performances and 2) how to determine the interactions between parameters that strongly affect the yield. Our transient sensitivity is adapted from a combination of two techniques: 1) Morris method [27] and 2) Sobol method [28]. Morris is used for process parameter reduction wherein process parameters may be cut down to a subset of parameters that are significantly related to the yield. On the other hand, the Sobol method is deployed for prioritization and weighting of the reduced process parameters.

1) Screening Method: Whereas AMS circuits are subject to different process variations, not all of them are critical to the performances metric of interest. Therefore, only parameter variations that have a significant impact on these performances should be considered for the yield estimation [29]. The key idea in this preliminary step is to relate the individual impact of parameter variations to the circuit performances variations and subsequently reduce the process parameters space by screening out the noninfluential parameter variations in the desired circuit performance. The detailed procedure for Morris-based process parameters screening is given in Algorithm 1. The first step is to generate a hyperspace identified by a d-dimensional l-level grid of the parameter variation intervals  $p_i = [lb(i), ub(i)] \forall i \in [1, d]$ , where d is the number of process parameters. The distance between two consecutive levels is given by  $\Delta$  (line 1). This hyperspace process parameter is then discretized through the scaled random sampling matrix referred to as the orientation matrix C (line 6) where  $J_{(d+1,d)}$  is a  $(d+1) \times d$  matrix with all ones,  $A_s$  is a  $(d+1) \times d$  sampling matrix defined for process parameters in the hypercube  $[0, 1]^d$ ,  $D^*$  is a d-dimensional diagonal matrix with elements  $\pm 1$  and finally,  $Pr^*$  is a  $d \times d$  random permutation matrix, in which each column contains one element equal to 1 and all the others equal to 0, with no more than one ones columns in the same position. The influence of the parameter  $p_s$  is then evaluated by performing  $N^*$ times runs, where we only change a single process parameter at a time between two successive runs of the circuit performance  $g_k$ . This process generates a trajectory of  $N^*$ points in the parameter space for which several elementary effects (EEs) at the different randomly selected values  $p_s$  are computed. Then, the EE, of the process parameter  $p_s$ , on the circuit performance  $g_k$ , is calculated for each  $s \in [1, d]$ (lines 5-8). Owing to the randomness of EE, we then characterize them using the mean  $\mu^*$  and standard deviation  $\sigma$ statistics. Based on these statistics, the algorithm computes sensitivity indices [also known as, global indices (GI)] in order to classify the parameters according to the Euclidian distance (line 12). Finally, the process parameter  $p_s$  (line 13) are classified according to their influence on the desired circuit performance.

Noninfluential parameters having negligible effects on the circuit performances that exhibit a low GI score

$$P^{n} = \left\{ p_{1}^{n}, \dots, p_{\hat{d}_{r}}^{n} \right\} \subset P = \{ p_{1}, \dots, p_{d} \}.$$
(14)

Influential parameters having large linear/nonlinear effects with/without interactions on the circuit performances that exhibit a high GI score  $P^i = P - P^n$ .

The proposed screening method will allow the removal of statistically insignificant process parameters (i.e., noncritical to the yield estimation) and thereby will reduce the yield analysis problem by the following ratio  $(d - \hat{d}_r/d)$ .

2) Parameter Prioritization: In this section, we aim to assess how the variation in the circuit performance can be apportioned to the different sources of variations in both electrical and physical circuit parameters which were identified in Section IV-B1 as influential parameters. To this end, novel measures should be introduced to quantify the circuit process parameters and the correlation thereof according to their influence on the AMS circuit performance.

Consider  $P^i$  the set of  $\hat{d}_p = d - \hat{d}_r$  influential process parameters which follow a certain distribution, and f(x) a circuit performance of interest depending on these parameters. It is assumed that f is a second order random variable  $f \in L_2(U^{\hat{d}_p})$ . Therefore, f has a unique SHD as detailed in Section III-A.

Owing to the orthogonality of the SHD, the variance of the circuit performance can be decomposed as

$$V(X) = V_X + \sum_{i=1}^{\hat{d}_p} V_i + \sum_{1 \le i \le j \le \hat{d}_p} V_{ij} + \dots + V_{1,2,\dots,\hat{d}_p}$$
(15)

where  $V_i, V_{ij}, \ldots, V_{1,2,\ldots,\hat{d}_p}$  denotes the partial variance with respect to a subset of the circuit parameters of the SHD  $X_i, X_{ij}, \ldots, X_{1,2,\ldots,\hat{d}_p}$  [defined in (5)], respectively

$$V_{i} = V(E(X|p_{i}))$$

$$V_{ij} = V(E(X|p_{i}, p_{j})) - V_{i} - V_{j}$$

$$V_{ijk} = V(E(X|p_{i}, p_{j}, p_{k})) - V_{ij} - V_{ik} - V_{jk} - V_{i} - V_{j} - V_{k}$$

$$\vdots$$

$$V_{1,...,\hat{d}_{p}} = V(f) - \sum_{i=1}^{\hat{d}_{p}} V_{ij} - \sum_{1 \le i \le j \le \hat{d}_{p}} V_{ij} - \dots$$

$$- \sum_{1 \le i_{1} < \dots < i_{\hat{d}_{p}-1} \le \hat{d}_{p}} V_{i_{1},...,i_{\hat{d}_{p}}-1}.$$

Therefore, the SHD is a rich means of analyzing the respective contribution of individual or sets of parameters to circuit performance variability. From the decomposition in (15), sensitivity indices  $(S_i, S_{ij}, \ldots, S_{1,\ldots,\hat{d}_p})$  can be naturally derived by normalizing the partial variances by V(X) to get the relation

$$1 = \sum_{1}^{d_p} S_i + \sum_{1 \le i \le j \le \hat{d}_p} S_{ij} + \dots + S_{1,2,\dots,\hat{d}_p}$$
(16)

where the order of the sensitivity indices  $S_i$  is equal to |i| = Card(i). Whereas, a more abstract characterization is required to replace the  $2^{\hat{d}_p} - 1$  contributions defined in (16) which leads to an intractable number of contributions as  $\hat{d}_p$  increases. To facilitate the characterization and hierarchization of the respective influence of each parameter  $p_i$ , we introduce new sensitivity indices: the main effect and the total sensitivity indices (TSIs). The TSI of a parameter *i*, denoted by TSI<sub>i</sub>, is defined as the sum of all sensitivity indices including all interactions effects involving parameter *i* 

$$TSI_i = S_i + S_{(i,\sim i)} = 1 - S_{\sim i}$$
(17)

where  $S_{\sim i}$  is the sum of all the  $S_{1,2,...,\hat{d}_p}$  associated to the different process parameters excluding the parameter  $p_i$ . Thus, the circuit parameter variations priorities are defined according to their importance through their TSI values. As a rule of thumb, parameters with TSI greater than 0.8 are considered as "very high priority," between 0.5 and 0.8 "high priority," and between 0.5 and 0.3 "less priority" in the next yield analysis stage [30]. The circuit influential process parameters set ( $P^i$ ) is therefore weighted according to these TSI values and denoted as weighted process parameters

$$P^{w} = \left\{ w_{i} p_{i} | w_{(i)} = \frac{\text{TSI}^{i}}{\sum_{j=1}^{\hat{d}_{p}} \text{TSI}_{j}} \right\}.$$
 (18)

## C. Transient Verification

In the previous stage of the methodology, we have performed transient SA to characterize the influence of process parameters on the circuit performances. The objective of this stage is to estimate the yield in light of the joint effect of the process variation and initial condition uncertainties. With the retrieved knowledge of the circuit sensitivity to its process parameters, the proposed yield estimation method should exhibit a full coverage of the parameters variation space. To do so, we generate a short and purposeful sampling scheme based on the weighted process parameters  $P^w$  defined in (18).

Recently, pattern matching techniques [31], [32] have emerged as first steps toward the automation of analog verification flows. As opposed to the traditional verification approaches wherein the circuit output is directly checked against the specification, pattern matching techniques study the similarities of the circuit output to its ideal behavior. These similarities are quantified in terms of quality measures reflective of how good the circuit is. The derived quality measures can be then used as new quantifiers of circuit failures and classifiers of circuits according to the safety criticality of their applications. However, state-of-the-art pattern matching methods suffers from the following shortcomings: 1) they are not suitable for verifying similarities between circuit behaviors that occur arbitrarily in order (i.e., present misalignment due to horizontal offset or different start-up time) which is the case of analog circuit and 2) they provide a single quality measure that falls short to handle multiple performances verification. To mitigate these limitations, a novel pattern matching technique is proposed in this paper.

1) Joint Recurrence Verification: Recurrence quantification analysis (RQA) is a technique developed by the nonlinear dynamic theory community to verify complex nonlinear systems [33]. In this section, we propose to use the RQA theory for the multiple performances verification of AMS circuits influenced by process variation uncertainties. To do so, we developed a variant from RQA technique called a joint recurrence quantification (JRV). The concept of this novel technique is to mitigate process variation in nonlinear AMS circuits as shown in Fig. 3. It aims to find recurrent patterns between an ideal/golden circuit output and multiple nonideal outputs in the presence of process variation by verifying their occurrence in their respective state spaces. In other words, it verifies if a state in the ideal output sequence recurs in the  $\varepsilon$ -neighborhood of the nonideal output sequence in the state space. Thus, it permits to develop recurrence quantifiers for both temporal and frequency domain properties of the circuit which allows the simultaneous verification of multiple performances and outputs. Unlike frequency domain analysis, JRV takes into account the initial conditions variation of the circuit. It also handles different natures of circuit behavior like transient and invariant behaviors in the same state space domain. Moreover, it can detect state changes in drifting circuits without necessitating any constraining assumptions on the output signal stationarity nor statistical distribution. Indeed, it depicts the different occasions when similar circuits states are attained even at distinct times.

Given the SSRE behavioral AMS circuit model, we first simulate the circuit under nominal design parameters to get the ideal expected transient circuit response denoted by  $x_{ideal}$ .



Fig. 3. Joint recurrence verification scheme.



Fig. 4. Illustration of the state space of an oscillator for three state variables.

We then simulate the circuit in presence of process variation in order to generate a set of nonideal transient responses of the circuit denoted by  $X_{nonideal}$ . The circuit transient responses are then mapped to their corresponding state space using a state space regeneration scheme (further details will be forthcoming). A visualization of the state space domain of the five stage ring oscillator circuit (see Fig. 7) defined by the node voltages at the state variables  $x_1$ ,  $x_4$ , and  $x_5$  is shown in Fig. 4.

Once the dynamics of both ideal and nonideal sequences are regenerated in the state domain, the reconstructed dynamics are thereafter verified using the JRV technique for a given radius threshold ( $\epsilon$ ); a distance matrix (called joint recurrence map), which represents the closeness of all possible state vectors pairs is then computed. Hence, the circuit outputs are mapped in a bi-dimensional space (the recurrence map), thus making it possible to identify time-recurrences that are not readily apparent in the original outputs by evaluating some specific measures. The main advantages of the proposed approach upon existing quality matching techniques is its ability to automatically handle horizontal offset, frequency offset, and start-up delay.

The implementation of the JRV technique is described in Algorithm 2. From the transient sensitivity stage of the proposed methodology, the circuit process parameters are associated with different weights according to their TSI. Therefore, a sampling procedure that draws appropriate parameter samples from this weighted process parameter set  $P^{W}$  is developed. The ultimate goal of this sampling strategy is to minimize the simulation effort while achieving full coverage of all possible circuit behaviors. Afterward, nonideal output sequences, denoted  $X_{nonideal}$ , are generated from the drawn process parameter samples (line 2).

To derive the matching quality between the ideal and nonideal output sequences, JRV consists of two main steps. The first step involves generating the circuit output in

## Algorithm 2 JRV-Based Method

- **Require:**  $P^w$ ,  $p_{nominal}$ , G, IC
- 1:  $x_{ideal} \leftarrow SSRE(p_{nominal}, mean(IC))$
- 2:  $X_{non-ideal} \leftarrow SSRE(P^w, IC)$
- 3:  $(\tau^i, d_{\rho}^i) \leftarrow Embedding \ dimension(x_{ideal})$
- 4: State space representation
- 5:  $y_{ideal} \leftarrow Time\_Delay(x_{ideal}, d_e^i, \tau^i)$
- 6:  $Y_{non-ideal} \leftarrow Time\_Delay(X_{non-ideal}, d_e^{ni}, \tau^{ni})$
- 7: Joint Reccurence matrix computation
- 8:  $JR(i,j) \leftarrow \Theta(\varepsilon \|y_{ideal}(i) Y_{non-ideal}(j)^1\|) \cdot \ldots \cdot \Theta(\varepsilon y_{pw})$  $\|y_{ideal}(i) - Y_{non-ideal}(j)^k\|), \forall k \in \mathbb{R}^d$
- 10:  $p^{\epsilon}(l) \leftarrow \sum_{m,n=1}^{N_{c}} \{(1 JR_{m-1,n-1}) \cdot (1 JR_{m+1,n+1}) \prod_{k=0}^{l-1} JR_{m+k,n+k} \}$ 11:  $RR = \frac{1}{N-k} \sum_{j-1=k} JR(i, j)$ 12:  $L_{max} = Max(n^{\epsilon}(l))$
- 12:  $L_{max} = Max(p^{\epsilon}(l))$
- 13:  $RP = -\frac{1}{\ln(T_{max})} \sum_{t=1}^{T_{max}} Y_{non-ideal}(t) \ln(Y_{non-ideal}(t))$ 14: **return**  $JRV_{metrics}$



Fig. 5. Time delay state space reconstruction procedure.

the multidimensional state space for each output sequence (lines 4–6). The algorithm reconstructs the different state space circuit responses according to Taken's theorem [34] for the computed embedding dimensions. This theorem states that it is possible to recreate a topologically equivalent state space representation of an original multidimensional system behavior using a single state variable, by means of the method of time delay [35] (lines 5 and 6). An illustration of the time delay method is shown in Fig. 5. The circuit behavior  $\varphi_t(u_i): \mathcal{S} \to \mathcal{S}$  evolves on a manifold  $\mathcal{M} \subset \mathcal{S}$ , with  $\mathcal{S}$  the circuit state space of dimension d and the circuit output at time  $t_n x_n = \text{SSRE}(u(t_n)) \equiv \text{SSRE}(u_n)$ . We define a delay reconstruction  $\phi : S \to \mathbb{R}^d$ , which is a composition of the circuit output  $x : S \to \mathbb{R}$  and an embedding procedure  $e : S \to \mathbb{R}$ . The delay embedding will map  $u_i$  through  $x_i = \phi(u_i)$  to  $x_i$ , and the embedding will have a trajectory  $\hat{\varphi}_t(x_i)$ .

During the dynamics regeneration, the time delay method needs the embedding lag  $\tau$  and the embedding dimension  $d_e$ parameters. These parameters are computed using the mutual information function [36] and the false nearest neighbors function [37], respectively. Once the circuit transient dynamics are mapped into the state space, we get the nonideal circuit state space dynamics  $Y_{nonideal}$  and the ideal state space dynamics yideal. The second step involves the study of the similarities/dissimilarities (recurring properties and patterns) between the nonideal state space dynamics of the circuit behavior in presence of process variation  $Y_{nonideal}$  against the ideal state space dynamics  $y_{ideal}$  (line 8). To do so, a tolerance parameter



Fig. 6. Relation JR matrix and circuit performances.

called threshold radius  $\epsilon$  is defined. This tolerance parameter specifies the maximum allowable deviation difference in terms of Euclidean distance between the two circuit outputs to be considered recurrent (i.e., same output value/state). The similarities is defined in a joint recurrence matrix JR (lines 7 and 8). It is computed as the Hadamard product of the recurrence matrix of the ideal circuit response and the recurrence matrix of the nonideal circuit response in light of process variation (line 8) according to the following equation:

$$\Theta(i,j) = \begin{cases} 1 & \text{if } \|y_{\text{ideal}}(i) - Y_{\text{ideal}}^k(j)\| < \varepsilon \\ 0 & \text{else} \end{cases}$$
(19)

where  $\Theta$  represents the Heaviside function. The obtained JR matrix locates the recurrent points whenever a similar state space behavior jointly occurs on both circuit output sequences  $x_{\text{ideal}}$  and  $X_{\text{nonideal}}$ . In other words, it checks if the state space trajectories  $y_{ideal}(i)$  at time *i* and  $Y_{nonideal}(j)$  at time *j* fall within the predefined threshold radius  $\epsilon$ . The patterns between the two output sequences are revealed by recurrence points and diagonal lines in the JR matrix. For instance, these diagonal lines represent periods in one output trajectory that follow similar parallel behaviors to those in another output. The closer the two outputs are, the more diagonal lines occur in the recurrence matrix. Subsequently, the frequency distributions of the diagonal lines lengths in JR are computed for each diagonal parallel to the main diagonal JR(i - j = r) for r equal to a constant (line 10). As an example, the JR matrix of two outputs of a five stage ring oscillator is shown in Fig. 6. Finally, the interplay between the circuit outputs is characterized by the following measures (lines 11-13).

- The RR which reveals the percentage of matching (i.e., the probability of the occurrence of similar state) in both circuit outputs.
- 2) The maximum joint sequence  $L_{\text{max}}$  that is the longest uninterrupted period of time that both circuits stay attuned.
- 3) RP which reflects the periodicity of the system in the state space; it has the ability to detect subtle changes in circuit responses such as the breakdown of regular periodic oscillation due to noise or process variation which are hard to detect using classical circuits analysis tools such as the Fourier transform or linear prediction.

a) Radius selection: How much recurrence we get in the JRV scheme depends on the value of the threshold parameter  $\epsilon$ . If the selected  $\epsilon$  is too small, there may be almost no recurrence points and the verification more likely fails. On the

## Algorithm 3 JRV Threshold Radius Computation

- 1:  $\mathcal{O} \leftarrow Compute\_Centroid (y_{ideal})$
- 2:  $D = \leftarrow Compute\_Distance (y_{ideal}, \mathcal{O})$
- 3: [maxRadius, maxRadiusIndex] = Max(D)
- 4:  $\epsilon_{optimal} = 0.05 * maxRadius;$

other hand, if  $\epsilon$  is selected too large, this entails a large false recurrence points due to the tangential motion (i.e., counting every coordinate in state space as recurrent) and thereby the verification will be biased. Hence, a particular attention should be paid to the choice of  $\epsilon$ . The question that arises is, "which values of  $\epsilon$  one should consider?". As each circuit has its own amplitude, the choice will be different for each application and it can also be extracted from the design specifications. In general, the value of  $\epsilon$  can be calculated according to the following algorithm.

The crux of Algorithm 3 is to determine the optimal tolerance threshold for any circuit output amplitude. To this end, a centroid O is computed using Green's theorem [38]. The threshold radius  $\epsilon$  is then chosen 5% of the maximum possible distance from the centroid of the circuit output attractor up to the boundary of that attractor (coordinates of the farthest point from centroid) as recommended in [33].

2) Multiple Hypothesis Testing: The goal of this step is to estimate the total yield rate for multiple performances in terms of the generated JRV metrics. On the one hand, the generated JRV quality metrics (RR,  $L_{max}$ , and RP) gives an idea of how close the circuit behavior to the ideal one, yet, each metric reflects a different circuit performance. On the other hand, these JRV measures are correlated and dependent and clearly a separate verification of this measures is not adequate as demonstrated in (9) (i,e., Poverlap fraction will be omitted and so the yield rate is over-estimated). Therefore, we use a statistical inference procedure and extend the statistical runtime verification scheme proposed in [39], which regards the verification of AMS circuits as a univariate hypothesis testing problem. The idea is to extend the statistical procedure to multiple decision making one in order to handle the simultaneous verification of multiple performance metrics: for each sample set of parameters, the procedure checks the JRV quality measures and gathers statistical evidence whether they satisfy the performance requirements (formulated as null hypotheses) based on the number of executions for which the performance constraints hold compared to the total number of executions. With such an approach, we do not need to estimate the overlay in acceptance region expressed in the overlap yield  $P_{\text{overlap}}$ . Hence, the total estimated yield rate will be directly assessed. Furthermore, the proposed simple yet elegant multiple hypothesis scheme allows a direct accurate multiple performance yield computation in a convenient way by controlling the tradeoff between computational burden and accuracy. In the sequel, we detail the proposed multiple hypothesis testing procedure. When conducting the yield estimation, the number of null hypotheses, m, is known in advance and corresponds to the number of performance metrics of interest G. However, the number of true and false null hypotheses  $H_{0_i}$ ,  $m_0$ , and  $m_1$ , respectively,  $m = m_0 + m_1$ , have to be determined. Table I summarize the possible outcomes when verifying *m* hypotheses simultaneously. A failure to

 TABLE I

 Multiple Hypothesis Testing Outcomes

	Passed	Failed	Total
Good Circuit	$\checkmark$	Т	m-R
Faulty Circuit	V	$\checkmark$	R
Total	$m_0$	$m_1$	m

compensate for multiple verifications can result in two types of erroneous inferences denoted by Type I error T and Type II error V as shown in Table I. When pursuing multiple performances verification, there is a potential increase in the chance of committing Type I errors  $(1 - \alpha)^m < (1 - \alpha)$ since  $\alpha \in [0, 1]$ . Hence, to guarantee an accurate yield estimation, the control of this type of error is highly recommended. Moreover, the JRV test statistics measures are dependent and correlated. For these reasons, we devise a scheme which minimizes V while accounting for correlations between the tests. To do so, we implemented a hypothesis testing scheme based on controlling the errors committed by falsely rejecting null hypotheses  $H_{0_i}$  denoted by false discovery rate (FDR) [40]:  $FDR = \mathbb{E}[(V/R)|R > 0] Pr(R > 0)$  where V is the number of false positive and R is the total number of rejected  $H_{0_i}$ . The detailed FDR-based procedure is summarized in Algorithm 4. First, we retrieve the metrics generated on the JRV stage. They are then used to define the null hypotheses that link them to the specification (line 1). This is followed by the computation of the standard score to determine the observed circuit JRV metric test statistic  $T_{obs}$  (loop between lines 3 and 9) for each performance metric  $g_i \in G$ . The next step is the non parametric FDR procedure as p-value adjustment repeated for N trials (loop between lines 10 and 25). We choose the p-value adjustment procedure because adjusted p-values permit a direct interpretation against a chosen significant level  $\alpha$  and so eliminate the need for lookup tables or knowledge of complex hypothesis rejection rules. The adjustment procedure starts by defining the acceptance and rejection regions under the assumption of  $H_{0_i} \in \mathcal{H}$  being true according to the type of test statistic (line 12). Then, the decision regarding whether each of the null hypotheses  $H_{0_i}$  holds or not is made. Thereafter, the FDR procedure is carried out in order to compute the false discovery proportion l. Afterwards, the number of actual rejection is corrected (line 21). Upon the rejection of one hypothesis  $H_{0_i}$  (i.e., violation of its corresponding performance metric  $g_i$ ), we increment the probability of failure counter  $N_{\text{failure}}$ . Finally, the yield is estimated in terms of the circuit failure probability as the percentage of samples with successful hypothesis over the total number of simulation runs (line 27).

## V. APPLICATIONS

In this section, we demonstrate the proposed parametric yield estimation approach on two benchmark circuits. All simulations were performed in MATLAB environment [41], on a Windows 10 operating system with an Intel Core i7 CPU processor running at 2.8 GHz with 24 GB of RAM.

## A. Ring Oscillator

We consider verifying a five-stage ring oscillator circuit as shown in Fig. 7. The performance metrics of interest

## Algorithm 4 FDR Controlling Procedure for Yield Rate Computation

**Require:**  $JRV_{metrics}$ , G,  $\alpha$ ,  $type\_test$ 1:  $\mathcal{H} \leftarrow$  set hypothesis( $G, JRV_{metrics}$ ) 2:  $N_{failure} \leftarrow 0$ 3: for  $i = 1 \rightarrow m$  do 4: for  $j = 1 \rightarrow N$  do 5:  $\mu_i \leftarrow \text{mean}(JRV_{metrics}(j, i))$  $\sigma_i \leftarrow \text{standard deviation } (JRV_{metrics}(j, i))$ 6: 7: end for 8:  $T_{obs}(i) \leftarrow \text{compute test statistic}(JRV_{metrics}(:, i), \mu_i, \sigma_i)$ 9: end for 10: for  $j = 1 \rightarrow N$  do 11: for all  $H_i \in \mathcal{H}$  do  $(A(j), R(j)) \leftarrow \operatorname{HT}(T_{obs}, type\_test, JRV_{metrics}, \alpha)$ 12: end for 13: 14:  $R = \sum R(j) = V + S$ 15:  $p_i \leftarrow \text{compute p-value } (H_i)$  $P \leftarrow sort(p_i)$ 16:  $l \leftarrow max\{p_i : P(i) \le \frac{i}{m} \frac{\alpha}{\sum_{i=1}^{m} 1/i})\}$ 17: for all  $k = 1 \rightarrow l$  do 18:  $H_{0_i} \leftarrow$ reject hypothesis  $H_{0_k}$ 19: end for 20:  $R_{corrected}(j) \leftarrow R - l$ 21: if  $R_{corrected}(j) \ge 1$  then 22: 23:  $N_{failure} \leftarrow N_{failure} + 1$ end if 24. 25: end for 26:  $p_{failure} = \frac{1}{N} \sum_{k=1}^{N} N_{failure}$ 

27: Yield 
$$\leftarrow 1 - p_{failure}$$



Fig. 7. Five stage CMOS ring oscillator.

TABLE II Specifications for Five Stage Ring Oscillator

Performance Metric	Specification
Oscillation frequency	$f_{nom} \pm 2\%$
Start up time	$\tau_{start\_up} \leq 35 \text{ ns}$

are the oscillation frequency and the start-up delay time (specifications are listed in Table II).

We consider process variations in the parameters of each nMOS and pMOS transistor. In addition, we take into account fluctuations in the power supply voltage  $V_{DD}$  and initial conditions. The process parameters in width W, channel length L, threshold voltage  $V_{\text{th}}$ , and the gate oxide thickness  $T_{\text{ox}}$  are introduced into each transistor  $M_i$ , i = 1, ..., 5 which results in 40 process parameters. By considering variations in initial



Fig. 8. Start-up time dependency on the initial conditions.

conditions and power supply voltage  $V_{DD}$ , the yield estimation problem rises to a 46-D problem. Consequently, our objective is to determine the yield of the circuit for these 46 random circuit parameters for the circuit specification given in Table II. Fig. 8 shows the transient simulation of the five stage ring oscillator for different initial condition (IC) values. Comparing the different start-up delay time, it can be observed that initial conditions have a strong effect on the start-up delay time. Indeed, by sweeping the initial voltages in the node voltages of the five inverters, the start-up delay time changes remarkably, especially for IC( $x_i$ ) =  $1e^{-4}V$  whereby the start-up time performance constraint is violated.

As a first step, we carry out our process parameters reduction and scoring scheme in order to estimate the impact of the joint effect of process variation and initial conditions variations on the ring oscillator performances. A Gaussian distribution with mean *m* fixed to nominal value and  $3\sigma$  variation is considered for each process parameter while a uniform distribution with 10% variation is adopted for initial condition variations. The Morris screening method was carried out for l = 10and  $N^* = 30$  to assess the sensitivity of the ring oscillator behavior to the above-mentioned process parameters. The highest mean  $\mu^*$  value identifies the most important process parameters. The order of importance is considered through the  $\mu^*$  ranking. In Fig. 9, a graphical representation of the ( $\mu$ ,  $\sigma$ ) Morris EEs is depicted for one of the five inverters process parameters. It can be observed in Fig. 9 that the Morris EEs identified five important parameters out of eight for each inverter, which reduces the yield estimation problem from 46-D to 31-D. Therefore, only these selected 31 parameters are chosen for the scoring scheme using the Sobol variancebased SA and later on for the verification scheme to estimate the yield rate. We carried out a Sobol global SA to relate the reduced set of parameter variations to the circuit performances variations. An illustration of the main and total Sobol sensitivity indices for one inverter parameters of the ring oscillation frequency is shown in Fig. 10. The SA results are in good agreements with the Morris sensitivity in Fig. 9. In fact, the variation in the sizes [width (W) and length (L)] of both pMOS and nMOS transistors and the threshold voltage  $(V_{th})$ have an impact on the circuit oscillation frequency. To score the importance of each of these circuit parameters, the amount of variation that is given by the main Sobol indices near one indicates that these parameters are more influential. Among all possible sources of process variations, the length L and threshold voltage  $V_{\rm th}$  are the dominant parameters with the highest



Fig. 9. Process parameters screening for ring oscillator.



Fig. 10. Process parameters prioritization for ring oscillator.



Fig. 11. Lmax variation with the transistors widths.

sensitivity indices 0.36 and 0.18, respectively. This can be justified by the random dopant effect [42]. Furthermore, a high correlation between parameters can be noticed through the gap between main and total effect indices. This is not surprising as the transistor threshold voltage fluctuation is directly related to the size of a transistor according to the following relation:  $\sigma V_{\text{th}} \propto (k/\sqrt{WL})$ . The obtained indices are used to guide the sampling selection in the JRV scheme in order to focus the verification on the parameters that affect the most the yield rate. The JRV setup parameters are as follows: embedding dimension  $d_e = 3$ , embedding delay  $\tau = 31$ , and the tolerated radius  $\varepsilon = 0.02$  ns.

The variation on the RR and maximum common sequence  $L_{\text{max}}$  computed using the proposed JRV scheme are shown in Figs. 11 and 12, respectively. Both the RR and the maximal joint sequence confirm the results reported in Fig. 10. In fact, they both fluctuate significantly while varying the design parameters, especially in the case of threshold voltage variation  $V_{\text{th}}$ . More particularly, the maximal joint sequence increases linearly with the transistor width (Fig. 11) and exponentially with the  $V_{\text{th}}$  (Fig. 13).

These obtained JRV schemes are used to assess the yield.

IC ranges	$x_i = 0.01, \forall i = 1, \cdots, n$							$x_i = 0.1, \forall i = 1, \cdots, n$						
IC Taliges	$x_5 \in [0, 0.5]$			$x_5 \in [0.5, 1]$			$x_5 \in [0, 0.5]$			$x_5 \in [0.5, 1]$				
	Yield Error Speedup		Yield	Error	Speedup	Yield	Error	Speedup	Yield	Error	Speedup	CPU		
	Rate	$\ .\ $	ratio	Rate	.	ratio	Rate	.	ratio	Rate	.	ratio	time [min.]	
MC	0.873	-	1×	0.884	-	$1 \times$	0.887	-	1×	0.891	-	$1 \times$	292.47	
LHS-MC	0.871	0.002	1.72×	0.881	0.003	1.77×	0.884	0.003	1.93×	0.889	0.002	$1.98 \times$	147.69	
QMC	0.878	0.005	$1.84 \times$	0.883	0.001	$1.98 \times$	0.889	0.002	$2.26 \times$	0.896	0.005	$2.32 \times$	126.06	
SA + QMC	0.884	0.011	3.54×	0.892	0.008	3.77×	0.898	0.011	4.61×	0.904	0.013	$4.95 \times$	53.07	
Proposed Method	0.896	0.023	8.43×	0.909	0.025	9.17×	0.911	0.024	$8.81 \times$	0.925	0.034	9.76×	29.97	

950

900

TABLE III YIELD ESTIMATION RESULTS FOR RING OSCILLATOR



Fig. 12. RR variation with the transistors widths.

The accuracy and efficiency of the proposed multiple yield analysis methodology are compared with those of primitive MC, and its variants namely, LHS-MC and QMC based on N = 1000 simulation trials. The verification was carried out under the confidence levels  $\alpha = 0.05$  and for initial conditions following a uniform distribution model. The primitive MC is considered as the base for the comparison in terms of speed-up and relative error. From Table III, the results of the three comparison show that the performance of the MC variants do not achieve significant improvement when compared to the primitive MC analysis method. Indeed, QMC is able to reach the MC golden result with around 2.1 speedup, while the MC+LHS method is  $1.85 \times$  faster than MC with approximately the same yield rate. This is due to the bad exploration of the process variation space during the sampling trials. Moreover, the ignorance of the high correlation effect between process parameters results in the ignorance of some special worst case combined effects. It can also be observed for the case of  $x_5 \in [0.5, 1]$  (columns 11–13) that our proposed method reduces the runtime up to  $9.76 \times$  in comparison with the conventional MC analysis, with no more than 3% relative error in estimated yield. It is also interesting to see that when the initial states get farther away from the equilibrium states, the circuit is subject to more failures and consequently, lower yield rates are obtained (columns 2-7). This can be explained by the direct dependency of the start-up time performance metrics on the initial conditions of the ring oscillator. For instance, when varying the initial conditions on the node voltages, the oscillation takes a longer time to settle when the initial conditions are too far from their dc values which is in good agreements with the results shown in Fig. 8.

SA approach is used during QMC with weighted parameter space according to the TSI weights obtained from the Sobol process parameter prioritization. The superiority of our proposed SA scheme combined with QMC over traditional QMC is demonstrated in line 7. In fact, the effective sampling according to the sensitivity indices

 $\mathbf{v}_{\mathbf{n}}$  at 850 600 750 0.42 0.4  $\mathbf{v}_{\mathbf{n}}$  0.36 8.5  $\mathbf{w}_{\mathbf{p}}$  $\mathbf{v}_{\mathbf{p}}$ 

Fig. 13. Lmax variation with the pMOS transistor width and threshold voltage.

TABLE IV SPECIFICATIONS FOR PLL DESIGN

Performance Metric	Specification
Lock-time	$t_{lock} \le 1.5 \text{ ms}$
Period jitter	$J_{period} \leq 5.62 \text{ ns}$
Stability	$\Delta_v \pm 0.05 \text{ V}$

enhances the yield estimation while the parameter screening enhances the verification runtime to more than  $2 \times$  comparing with QMC.

## B. Phase-Locked Loop

PLL-based circuits are key mixed-signal building blocks widely used in various applications. It is essentially a closedloop feedback system with a challenging highly nonlinear behavior. A simplified block diagram of a PLL-based frequency synthesizer is depicted in Fig. 14. In practice, simulation is the common practice for the verification of the PLL to its desired performances [43]. However, several limitations of classical s-domain analysis based on a continuous-time approximation of PLL operability have been reported in [44]. For instance, classical linear analysis is not rich enough to describe many crucial and hidden dynamics due to the following two reasons: first, it does not comprehend the sampling nature due to the discrete-time operation of the phase frequency detector. Therefore, it can result in a degraded performance particularly in terms of jitter peaking. Second, since s-domain analysis is a steady-state analysis it does not predict the nonlinear acquisition process of the PLL. The PLL under verification needs to satisfy the performance requirements given in Table IV to avoid yield loss.

In this application, we consider the most dominant noise in PLL designs stemming from shot noise in the VCO block and manifesting itself as accumulation jitter (also known as FM jitter) [45]. The noisy VCO output due to the intrinsic jitter is

			$\alpha =$	0.05			$\alpha = 0.01$						
	Case I: Without jitter			Case II: With VCO jitter			Case I: Without jitter			Case II: With VCO jitter			
	Yield Error Speedup		Yield	Error	Speedup	Yield	Error	Speedup	Yield	Error	Speedup	CPU	
	Rate	.	Ratio	Rate	.	Ratio	Rate	.	Ratio	Rate	.	Ratio	time [min.]
MC	0.9531	-	1X	0.8972	-	1X	0.9386	-	1X	0.8806	-	1X	1510.27
LHS-MC	0.9543	1.2e-3	1.78X	0.8985	1.3e-3	1.82X	0.9403	1.7e-3	1.58X	0.8825	1.9e-3	1.72X	878.06
QMC	0.9547	1.6e-3	2.23X	0.8980	1.8e-3	2.46X	0.9405	1.9e-3	2.17X	0.8826	2e-3	2.23X	677.25
SA+QMC	0.9550	1.9e-3	5.62X	0.8993	2.1e-3	5.79X	0.9409	2.3e-3	5.28X	0.8829	2.3e-3	5.71X	264.50
Our Method	0.9559	2.1e-3	9.87X	0.8998	2.6e-3	11.53X	0.9413	2.7e-3	9.16X	0.8817	2.9e-3	10.94X	138.05

 TABLE V

 PLL YIELD ESTIMATION RESULTS FOR DIFFERENT CONFIDENCE LEVEL



Fig. 14. Conventional PLL frequency synthesizer.



Fig. 15. Recurrence periodicity for different damping factors.

afflicted according to the following Equation:

$$\operatorname{Out}_{\operatorname{VCO}} = A \, \cos\left(\omega_0 t + K_V \int_0^t \frac{\operatorname{Out}_{\operatorname{LPF}}(\tau)}{1 + J\theta \frac{K_V \operatorname{Out}_{\operatorname{LPF}}}{2\pi}} d\tau + \phi_0\right)$$
(20)

where J stands for the jitter deviation,  $K_V$  is the VCO gain, Out<sub>LPF</sub> is the filter output,  $\phi_0$  is the initial phase, and  $\theta$  a zero mean unit-variance Gaussian random process.

We performed our JRV scheme on the PLL application for an embedding dimension  $d_e = 3$  and an embedding lag  $\tau = 15$ . Fig. 15 plots the RP for different damping factors  $(\xi_1 = 0.1, \xi_2 = 0.5, \text{ and } \xi_3 = 0.707$ , respectively). It can be noticed that a longer settling time is required for the PLL to achieve lock when  $\xi$  increases. In fact, for  $\xi_3 = 0.707$  (red line in Fig. 15) higher RP values are attained than those for  $\xi_1 = 0.1$  and  $\xi_2 = 0.5$ . This means that the PLL presents less periodic outputs. In fact, the closer its value to 0, the closer the PLL is from its ideal behavior. In addition, the variation of the VCO jitter with the RP shows an exponential increase for values greater than 5.62 ns.

The resulting JRV metrics are employed in the global hypothesis testing scheme for different confidence levels  $\alpha = 0.05$  and  $\alpha = 0.01$ . In this application, the JRV metrics

 $(RR, L_{max}, and RP)$  are employed in the global hypothesis testing scheme for different confidence levels  $\alpha = 0.05$  and  $\alpha = 0.01$ . The obtained parametric yield results are shown in Table V and compared to the MC method and its variants in light of process variation and jitter uncertainty. To demonstrate the efficiency of the proposed SA scheme, we have used the reduced weighted process parameters list to generate LDS coordinates for QMC method (line 7 in Table V). It can be seen that our SA combined with QMC can achieve better yield estimates with more than 2.5× speed-up compared with QMC. This is thanks to the process parameter screening method. Clearly, parameters variation elimination enhances the QMC efficiency in which yield estimation is not performed for noninfluential parameters. Moreover, sampling the relevant region of the parameter space based on the sensitivity weights significantly improves yield estimation efficiency. The presence of process variation alone has shown higher yields. However, the yield rates considering jitter disturbance and process variations have shown lower rates (columns 5 and 11). It is obvious that the combined process variation/jitter effects will result in more PLL failures due to the high sensitivity of the VCO to noise disturbances. In order to show the dependency of the yield assessment results on the confidence level  $\alpha$ , yield rates for  $\alpha = 0.05$  (columns 2–7), and  $\alpha = 0.01$  (columns 8–13) are computed. It is obvious that in the case  $\alpha = 0.01$  slightly lower yield rates are obtained (column 8) compared to those reported for  $\alpha = 0.05$ (column 2). Indeed, the multiple hypothesis testing results can be different for different confidence levels and the yield accuracy would be a very small degree different (less than 0.003%). In short, the hypotheses tests results can be slightly different for different confidence intervals and the accuracy would be compromised if the confidence level is too high or too low. Lower confidence level would increase the rejection; Higher confidence level on the other hand would increase the error margin and degrade the accuracy. A significant simulation-time saving (more than  $10 \times$  reduction) resulting from using our proposed methodology has been remarked. The savings come from two distinct mechanisms. First, the SA approach: 1) reduces the process parameters dimension space; 2) prioritizes the parameter variation selections according to their influence on circuit performances; and 3) reveals hidden worst performances due to interactions between different parameters variations. Second, the multiperformances yield estimation scheme is conducted simultaneously through a global hypothesis testing procedure. On the contrary, multiple single performances simulations runs are performed using MC which results in an over-estimated yield due to the correlated PLL performances wherein rejection regions overlap.



Fig. 16. Effectiveness of our proposed approach.



Fig. 17. Effectiveness of the proposed screening method.

The relative yield estimation error with respect to the number of simulation runs of the primitive MC and the proposed method are compared in Fig. 16. The relative small number of the required simulations runs shows the efficiency of our approach, by which it was possible to have at least a  $9 \times$ computational cost gain without paying in terms of accuracy.

## C. Discussion

To corroborate the process parameter reduction results obtained using the Morris sensitivity method, we perform an MC simulation on the reduced and nonreduced process parameters set. The aim of this experiment is to confirm that the nonsignificant parameters identified through the Morris method do not actually significantly affect the yield results. Fig. 17(a) compares the yield rate estimate using primitive MC simulations before and after process parameter reductions for ring oscillator and PLL design.

The obtained yield rates fully confirms the Morris results, since for both applications the estimated rates account for less than a maximum of 2% error. This confirms the capability of our proposed process parameters screening approach in (1) identifying the actual nonsignificant parameters variation on the circuit performances of interest (2) notably reducing simulation runtime [see Fig. 17(b)] by removing redundant non statistically significant simulations as compared to the primitive MC without considering the reduction for both PLL and ring oscillator circuits.

## VI. CONCLUSION

In this paper, a methodology which enhances the capability to predict multiperformance variability-aware parametric yield estimation for nonlinear AMS circuits is proposed. The approach is based on global SA to reduce and prioritize the process variation space due to 65 nm technology node. This permits to cut down on simulation time and to perform a more holistic, comprehensive, and accurate yield analysis. The acquired sensitivity results are efficiently embedded in a JRV scheme of the AMS circuit behavior. The multiperformance yield estimation problem is then cast as a single statistical problem under the limiting conditions retrieved from the prescribed specifications. Experimental results show that our methodology prevails over MC techniques in yield rate assessment. It has demonstrated up to 11× computational reduction capability while retaining accuracy.

In its present form, the methodology considers only process variations. These spatial unreliability effects can be immediately detected right after fabrication. Temporal unreliability effects, on the contrary, vary with the time and the operating conditions (e.g., the operating voltage and temperature). Hence, they are extremely hard to detect and cannot be fixed nor recovered. Future improvements of this paper may include modeling and verifying AMS circuits reliability to these temporal effects. More specifically, aging effects (negative-bias temperature instability) and transient effects [46] (single event transients).

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