Run-Time Hypothesis Testing of Analog Circuits in Presence of Noise and Process Variations

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Abstract

Today's analog/RF design and verification face significant challenges due to circuit complexity and short market windows. In particular, the influence of technology parameters on circuits, and the issues related to noise modeling and verification still remain a priority for many applications. Noise could be due to unwanted interaction between the circuit elements or it could be inherited from the circuit elements. In addition, manufacturing disparity influence the characteristic behavior of the manufactured circuits. In this report, we discuss a methodology for modeling and verification of analog/RF designs in the presence of noise and process variation using statistical run-time verification technique. In order to study the statistical behavior of noise, our approach is based on modeling the designs using stochastic differential equations (SDE), an extension to ordinary differential equations (ODE) with stochastic properties that are suited for modeling a continuous systems in time domain. Then, we define a run-time based verification method combined with process variation, integrated in the SDE simulation framework for monitoring properties of interest in order to quickly detect errors.

Contents

1 Introduction

In recent years, advanced technologies have allowed designers to develop smaller, faster, low power analog/digital/RF designs in a single chip, known as systems-on-a-chip (SoC). This complex integration among various blocks has made the design and verification a cumbersome process, mainly due to nonlinear dynamics of the design, interdependency of the state variables, and the need for a continuous infinite state-space analysis. Additional effects such as noise, fluctuations, and technology variations have also influenced the quality and yield of the manufactured circuits [19].

Noise is a random phenomena whose origin has been studied by many researchers for decades. The sources of noise could be due to unwanted interaction between the various design blocks (ex: cross-talk noise) or it could be inherited from the circuit elements (ex: thermal, shot and flicker) [6]. Further noise classification such as *phase*, *jitter* or *device switching* falls within the functional characterization of the design and are influenced by both inference and inherited noise.

Thermal noise is associated with the random thermal motion of carriers in a material, and the extent of the motion is proportional to the resistance of the material and its absolute temperature T. It also exists whenever there is a presence of conducting channel and its influence become nullified as T approaches zero [6]. *Shot noise* is generally found in junction semiconductors, although it was originally observed in vacuum tubes, its existence is attributed by the random flow of current across the potential barrier. For instance, in a semiconductor p-n junction, the movement of charge carriers into the depletion region generates a small pulse, that contributes to shot noise. Effective at lower frequencies the *1/f* noise also called as *flicker noise* is due to impurities in a conductive channel that are caused due to varying doping concentration [6]. Flicker noise is a general form of a power law noise or a $1/f^{\alpha}$ noise where α is considered to vary between 0 and 2 [6]. *Cross-talk* noise, is due to capacitive and inductive coupling between the lines that run close to one another, meaning, the signal on one line will influence the behavior of the signal in the adjacent lines. This kind of interference effect depends on the frequency of the signal, the proximity of the two lines, and the total distance that the two lines run adjacent to one another [15].

The question now is *Can we eliminate noise?* It depends on the type of noise and its origin. For instance, with proper layout and shielding techniques between the two neighboring lines in a design, interference noise can be nullified [6]. On the other hand, the inheritance noise can be reduced and cannot be eliminated completely. This is because, the dynamics of such noise are influenced by the way active/passive elements are manufactured, environment constraints (such as fluctuations, temperature) that could totally alter its behavior.

Things get even more challenging when we look at the different steps involved in fabricating a circuit. This is because, manufacturing steps present a completely different set of constraints on the designs. For instance, in a MOS transistor, can we assume the ultra-thin oxide layer that separates the gate from the channel has a smooth edge? Absolutely not, because, we cannot control the manufacturing process entirely [5] and hence will create disparities at different points in a device. Such discrepancies, will make the MOS transistor susceptible to varying tunneling phenomena, thereby altering

the characteristics of the noise [29].

The sources of variations due to fabrication can be classified as *interdie* and *intradie* [12]. While, *interdie* variation also called as *global* variation assumes the device/circuit parameter discrepancies to be the same across *die-to-die* or *lot-to-lot* or *wafer-to-wafer* [12], *intradie* also called as *local* variation reflects the mismatch in a component with reference to a adjacent component [12]. In this case, the devices in the same circuits might have different variations, thereby posing a serious threat on circuit performance and functionality. So, the optimum approach for the circuit design is to recognize the degree of freedom allowed and the availability of different devices within the technology.

The next step is to understand the kind of quantification required to study the effect of noise and process variation. For any design influenced by noise, the variation of input/output signal amplitude (voltage, current etc.) is considered random with time. An important noise metrics (signal-to-noise ratio (SNR), noise figure (NF)) for such random signals would be to measure the root mean square (RMS) in terms of probability density function (PDF). SNR is a measure used to determine the quality of a signal that are corrupted by noise, and NF is a quality measure of SNR degradation. More often, we may also be interested in finding the worst-case scenario of noise voltage/current in terms of its peak-to-peak amplitude. Hence, based on probability density function with a known standard deviation, one can translate the RMS noise voltage/current to its counterpart peak-to-peak voltage/current.

Today's circuit simulation use statistical modeling to study the effect of process variation and noise on analog/RF circuit performance [16]. Such standard statistical compact SPICE [16] models allow many deep-submicron process variation on device parameters to achieve a good fit between measured (SNR, NF) and extracted values. But, at circuit level, statistical analysis that involves studying the PDF can be time consuming and can also suffer from memory space problems [15] due to increases in higher order harmonics.

Generally, designers use *Worst Case* or *Monte Carlo* methods [2] to study the effect of process variations. In Worst-Case analysis, analog circuits are modeled with pessimistic process corners. This worst-case variation are determined in the foundry design document, and are based on $\pm 3\sigma$ parameter distribution. For a given circuit, and for each components, process corners are constructed to maximize/minimize one specific performance of a device (e.g., speed, power, area, etc.). The main advantage of such simulation techniques is its ability to achieve robustness and sensitivity to the worst-case scenario and can provide much faster simulation results [17]. But, such analysis that targets single device variation has to be always compromised with other parameter variation, meaning, its does not provide leverage for additional parameter variation. Such complex analysis may increase the design efforts and costs.

Monte-Carlo methods take into account a predefined distribution (usually normal distribution) of the device parameters due to process variation. When defining normal distribution, the designers has to use certain standard deviation, usually, it is $\pm 3\sigma$ parameter distribution. This means that, unlike worst-case that target for single device performance, monte-carlo methods use repeated simulation technique for multiple device performance [17]. In the end, it provides a statistical estimate of the analysis with

certain confidence level. Though, it looks attractive, monte-carlo simulation may or may not always use worst-case parameter variation for devices and iterative in nature.

An alternate solution to the problem of expensive simulation times and memory usage would be to capture the behavior of the design as a purely mathematical or numerical model [22], [21] and integrate process variation on device parameters. In that case, one has to provide a way to handle the error bounds on the results. For noise and process variation, rather than qualitative estimation of the design specification, like SNR, NF, and so on, we might be interested in the functional evaluation of the circuit. For instance, a designer would like to monitor the functional behavior (current, voltage) at run-time, and then comparing it to the expected result. This leads us to statistical behavior rather than detailed response of the system. Therefore we propose to use stochastic differential equations (SDE) [3] as an analog/RF noise model. However, the challenge is to incorporate verification techniques that are suited for SDE based modeling.

In recent years, formal and semi-formal methods have been advocated by many research groups and industries for analog and mixed signal verification [8]. In particular, run-time verification techniques have been shown to be effective in detecting violation of the design specification thereby avoiding exhaustive checking inherited by traditional circuit simulation and formal methods. Run-time verification employs logical monitors to check (*online* or *offline*) if an execution (simulation) of the design model violates the design specifications (properties).

Statistical run-time verification combines hypothesis testing [27] and Monte Carlo simulation for monitoring the properties in an analog circuit. Hypothesis testing is the use of statistics to determine the probability that a given hypothesis is true and in general, expressed as a null hypothesis *H0* and the alternative hypothesis *H1*. The statistical property, is expressed as a null hypothesis, while the alternative hypothesis becomes the counterexample. For noise and process variation, the designers might be interested in evaluating the statistical behavior (such as confidence interval, error margin, reliability, etc.) of the circuit.

The first step in hypothesis testing is to understand the distribution of any parameters (observations) that are used in the analysis. For instance, designers may wish to estimate the error margin involved in the analysis of the *jitter period* at the VCO output. This can be accomplished by observing the information along the simulation path as a sample with a predefined distribution. This kind of estimation involves statistical techniques such as evaluating the parameters based on the sample mean, confidence interval, hypothesis testing, and modeling (e.g., regression and density estimation) [27]. In order to achieve a high confidence interval and error margins, the design has to be evaluated for different trajectories.

The rest of the paper is organized as follows: In Section 3, we overview the theory and modeling of analog/RF designs using SDEs. In Section 4, we introduce the proposed methodology for monitoring noise in analog/RF designs. Experimental results are illustrated in Section 5, followed by discussions and conclusion in Section 6.

2 Related Work

Lately, several new techniques that targets analog/RF designs have been developed by many research and industrial groups. For instance, in [28] the authors have numerically evaluated an electronic oscillator based on a new physical descriptions of thermal noise. The method involves combining the non-equilibrium statistical mechanics with the SDE based Langevin approach. But, the method fails to neglects non-linearity and also ignores the process variation. Methodology based on closed-form solution of SDE's has been introduced in [26], where the effect of noise has been analyzed for a single-ended input differential amplifier. As discussed earlier, such analytical approach of solving SDE's using stochastic calculus are limited to circuits that have closed form solution and is not accurate enough to conclude on the results. Similarly, the proposed transient noise analysis in [4] enables circuit designers to efficiently perform SPICE-accurate device noise analysis on complex non-periodic analog/RF blocks. However, such noise analysis at low level of abstraction is time consuming. Also, Synopsys has introduced a tool, HSPICE RF [11] implementing stochastic differential equation (SDE) techniques to make a direct prediction on the statistical behavior of analog/RF circuits. The results of such a simulation include the usual deterministic transient analysis waveforms, and also its time-varying root-mean square (RMS) statistical behavior. Similarly, an open source tool, fREEDA [9] provides a leverage to model and analyze noise using SDEs. Based on fREEDA, the authors in [13] have performed an SDE based phase noise simulation in time domain. Though the phase noise is accurately predicted for a fairly large frequency range, their technique suffers from long simulation run-times without the mean to be able to detect undesired behavior.

Many methodologies have been proposed by different research groups and the details are provided in our research proposal. Lately, in [30], the authors propose a runtime verification methodology for statistical properties of analog and mixed signal (AMS) designs in an offline fashion. The approach combines system of recurrence (SRE) equation AMS model with the statistical method and Monte Carlo simulation to verify the statistical property. The above approach has two problems: 1) SRE models are based on if-then-else structure and is not accurate. 2) The method also fails to address the issue related to noise and process variation.

In common practice, there are several methodologies to verify quantitative and probabilistic properties in a real-time system at runtime. However, providing a common platform that could study the effect of noise and process variation for monitoring the statistical property in an analog circuits has not been addressed.

3 Preliminaries

3.1 Stochastic Differential Equation

A SDE is an ordinary differential equation (ODE) with stochastic process that can model unpredictable real-life behavior of any continuous systems [3]. A stochastic process is a collection of random variables $\{X_t;\ t\ \epsilon\ T\}$ defined on a given probability space indexed by the parameter time t that vary over an index set T. The random term

in SDE can be purely additive or it may multiply with some deterministic term [3]. For Example, consider the population growth model describe by the following differential equation

$$\frac{dN}{dt} = a(t)N(t); \quad N(0) = A \tag{1}$$

where *N(t)* is the size of the population at time *t*, and *a(t)* is the relative rate of growth at time *t* and *A* is some initial constant. But, *a(t)* is unknown and is random in nature. Hence a reasonable mathematical interpretation of the randomness for the above equation can be described as

$$\frac{dN}{dt} = a(t)N(t) + \xi_t N(t); \quad N(0) = A \tag{2}$$

The term *a(t)N(t)* is the deterministic drift coefficient while the term $\xi_t N(t)$ represents the stochastic effect [3]. However, in SDE terminology, the above equation can be represented in two forms: *Itô* or *Stratonovich* [3] for more mathematical explanation of *Stratonovich* form. If we consider ξ_t to be the pathwise derivative of Brownian motion (or Wiener Process) dB_t, then Equation 2 can be written in *Itô* differential and integral form as given by

$$\begin{aligned} dN &= a(t)N(t)dt \qquad &&+N(t)dB_t \\ N &= \int_0^t a(s)N(s)ds \quad &&+\int_0^t N(s)dB_s \end{aligned} \tag{3}$$

However, to solve Equation 3 traditional calculus lack the structure to handle stochastic process, and hence we need special mathematical interpretation in the form of stochastic calculus to solve the equations involving brownian motion [3]. A Brownian (or a Wiener process) is a family of random variables W_t, indexed by nonnegative real numbers *t*, defined on a common probability space with the following properties:

- $W_0 = 0$.
- With probability 1, the function $t \rightarrow W_t$ is continuous in *t*.
- The process W_t has stationary, independent increments.
- The increment W_{t+s} - W_s has the Normal(0, t) distribution.

In addition, stochastic calculus uses the concept of expectation and *Itô* isometry to solve SDEs. Expectation determines the behavior of any system in the absence of randomness and hence it is easy to conclude that the expectation of any random process (Brownian or Wiener) is zero. As brownian motion cannot be solved using definite integral, the goal of *Itô* isometry is to replace the brownian motion $dB_s$by deterministic term *ds* for solving SDEs.

In contrast, there is not always a closed form solution for SDEs, hence researchers have looked for solving them numerically. The methods based on numerical analysis are reported in [18], which involve discrete time approximation in a finite time interval over the sample paths. The simplest time discretization approach is based on *Euler-Maruyama* approximation [18] which we adopt in this report.

Consider an *Itò* SDE in differential form

$$dX_t = a(X_t)dt + b(X_t)dW_t \tag{4}$$

where a and b are some function of time and W_t is a Wiener process. Based on *Euler* approximation, equation (4) can be written as:

$$X_{n+1} = X_n + a(X_n)\Delta_n + b(X_n)\Delta_n \Delta W_n \tag{5}$$

where for time step τ,

$$\Delta_n = \tau_{n+1} - \tau_n; \;\; \Delta W_{\tau n} = W_{\tau n+1} - W_{\tau n}; \tag{6}$$

for *n=0,1,2.....N-1* with initial value $X_0 = x_0$; and for maximum N simulation steps.

The recursive method described by equations (5) and (6) gives only an approximate solution and it is important to note that the solution is close to the *Itò* process [18]. The amount of deviation of the numerical solution is defined by the *absolute error* which satisfies the convergence properties.

In summary, the role of numerical approximation is to model and simulate a given design in an iterative fashion. More accurate numerical methods such as *Milstein, Taylor, Runge-Kutta* are available in [3] for the simulation of the analog/RF designs.

3.2 Hypothesis Testing

Hypothesis testing is the use of statistics to determine the probability that a given hypothesis is true. Hypothesis testing in general, has two parts:

- *Null hypothesis*, denoted by H_0, which is what we want to test (e.g., *jitter_period* $\leq$ *3.2 ns*); and
- *Alternative hypothesis*, denoted by H_1, which is what we want to test against the null hypothesis (e.g., *jitter_period* $>$ *3.2 ns*).

The statistical property, is expressed as a null hypothesis, while the alternative hypothesis becomes the counterexample. For noise and process variation, the designers might be interested in evaluating the statistical behavior (such as confidence interval, error margin, reliability, etc.) of the circuit. The first step in hypothesis testing is to understand the distribution of any parameters (observations) that are used in the analysis. For instance, designers may wish to estimate the error margin involved in the analysis of the *jitter period* at the VCO output. This can be accomplished by observing the information along the simulation path as a sample with a predefined distribution. This kind of estimation involves statistical techniques such as evaluating the parameters based on the sample mean, confidence interval, hypothesis testing, and modeling (e.g., regression and density estimation) [27]. In order to achieve a high confidence interval and error margins, the design has to be evaluated for different trajectories.

If we reject H_0, then the decision to accept H_1 is made. The conclusion is drawn with certain probability of error (α and β) along with specific confidence level. Usually, α, also called the *significance level*, denotes the probability of rejecting H_0 when it is

actually true (Type I error) and β denotes the probability of accepting H_0 when it is actually false (Type II error). For instance, $\alpha = 0.05$ and $\alpha = 0.01$ refer to the confidence level of 95% and 99%, respectively. The question now is *how to decide on rejecting the null hypothesis H_0?*

In hypothesis testing, if the observed sample data over a given interval is within some critical region, then we reject the null hypothesis H_0, also known as the rejection region. The critical region depends on the distribution (*lower tail, upper tail* or *both tails*) of the data under the null hypothesis, the alternative hypothesis, and the margin of error. If a large value of the test statistic would provide evidence for rejecting H_0, then the rejection region is in the upper tail of the distribution of the test statistic else the rejection region is in the lower tail of the distribution.

3.3 Process Variation on Device Parameters

In following, we discuss the influence of *0.18μm* process technology on device parameters that will be adopted in this research. However, the effect of process variation for other technologies can be extended easily.

Influence of *0.18μm* Process Variation on Resistor. Poly resistor that are built with poly layer deposited over field oxide is used widely to represent resistors in analog/RF designs and its value depends on the sheet resistance (R_{sh}) associated with the poly layer. For a given process the variations in poly resistance are mainly due to fluctuation in film thickness, doping concentration, doping profile and annealing conditions [12]. Usually, a *0.18μm* CMOS process allows 10 to 15% variation in poly thickness which attributes to a similar variation on poly sheet resistance R_{sh}. In addition, there is a 10 to 20% variation in R_{sh} due to doping and ion implantation steps. By large, *0.18μm* CMOS allows 15 to 25% variation in sheet resistance due to the deviation in poly thickness and doping concentration [29]. For instance, the sheet resistance R_{sh} for TSMC *0.18μm* process is $7.9\Omega/square$ [1]. This means that, for the *slow, nominal* and *fast* process corners, the variation in sheet resistance R_{sh} would be 15%, 20% and 25% respectively. This allows us to use three different values for the resistors in an analog/RF circuit.

Influence of *0.18μm* Process Variation on Capacitor. A typical MOS transistor can be used as a capacitor when operating in the linear region, with the gate representing one plate and drain/source with the channel forming the other plate. Apart from MOS capacitors, current CMOS technology provides *poly-to-poly* capacitors, *metal-to-metal* capacitors and *junction* capacitors. We consider the effect of MOS capacitance in *0.18μm* process, where the variation in MOS capacitance is mainly due to the variation in oxide thickness and the channel doping concentration across the die/wafer. For a *0.18μm* process, a $\pm$20% variation has to be taken for MOS capacitance which represents a deviation of +20% for *slow* process corner and -20% for *fast* process corner with no changes in capacitance value for *nominal* process corner. However, variation in metal-insulator-metal (MIM) capacitor can be more than 20% [12]. For a given capacitor, a variation of $\pm$20% in the capacitance value is used to represent a *fast* and *slow* process corners.

Influence of *0.18μm* Process Variation on MOS Transistor. A typical MOS transistor can be classified as *enhancement-n* type or *enhancement-p* with positive or negative threshold voltages respectively. For a given technology, the process variation in a MOS transistor may cause a deviation in threshold voltage (V_t), length and width of the transistor (L and W), oxide thickness (T_{ox}) which results in the change in device characteristics across the die/wafer. The deviation in threshold voltage V_t and transconductance parameter K is calculated as [29]:

$$\begin{array}{rl} \sigma(\Delta V_t) & = \frac{A_{VT}}{\sqrt{WL}} \\ \sigma(\frac{\Delta K}{K}) & = \frac{A_K}{\sqrt{WL}} \end{array} \tag{7}$$

We consider the *0.18μm* process variation in threshold voltage V_t and transconductance K. For instance, given an analog/RF circuit that involve the use of MOS transistor, the variation in threshold voltage is calculated based on equation(7) and is passed as a *slow, nominal* and *fast* process corner parameter in the verification environment. Table 1 summarizes the technology parameters needed to calculate V_t and K.

Table 1: CMOS *0.18μm* Process Variation

Type	$\mathbf{A}_{VT}$ [$mV\mu m$]	A_β [%μm]	$\frac{g_m}{I_{DS}}$ [$\frac{S}{A}$]	($\mathbf{V}_{GS}$ - $\mathbf{V}_T$) [V]
nMOS	5	1.04	2.08	0.96
pMOS	5.49	0.99	1.80	1.11

4 Statistical Run-Time Verification

Figure 1 shows the overall statistical run-time verification methodology. Thereafter, given an analog design described as a system of *ODEs*, the idea is to generate SDEs that describes the noise behavior. For process variation, the technology vendors create a library of devices with different corners [29] that characterize the device in terms of power, speed, area, etc. This allows the designers to choose from a range of devices based on the application and requirements. In our proposed methodology, for 0.18μm process and with a known $\pm 3\sigma$ deviation, different circuit parameters are derived using gaussian distribution as described in Algorithm 1.

For a *0.18μm* CMOS technology, we have to account for 15 to 25% variation in sheet resistance in order to study the effect of process variation [29], i.e., the sheet resistance R_{sh} is 7.9$\Omega/\square$ [1]. This means that, for the process corners, the variation in R_{sh} would be 15%, 20% and 25%, respectively. Typically, $\pm$20% variation is taken for capacitance due to *0.18μm* process [29].

The SDE model, process variation, along with the statistical properties, and the environment constraints are evaluated using Monte Carlo monitors in an statistical run-time verification environment.

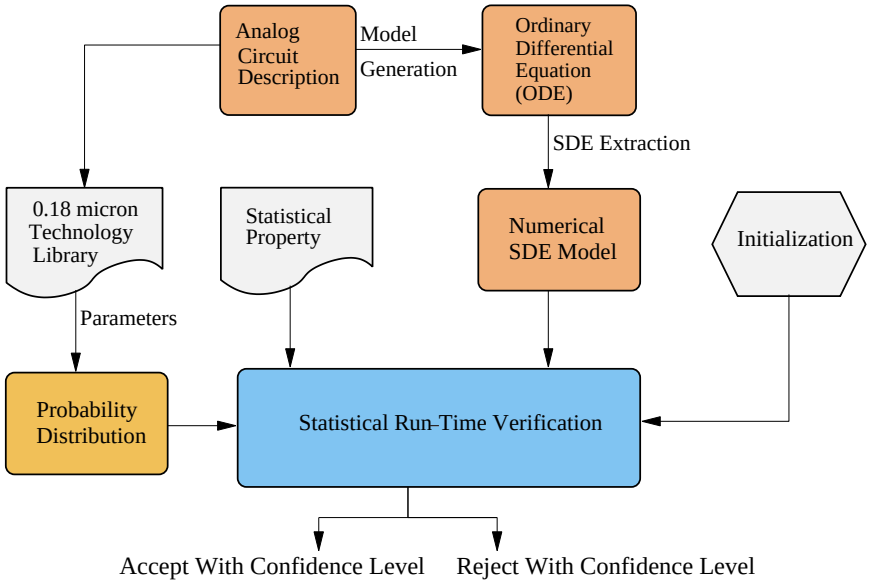


Figure 1: Statistical Verification Methodology

The basic idea behind the Monte-Carlo method is to simulate the SDE model for multiple trajectories and sample them in order to calculate the desired statistics for a given confidence level δ. For instance, for K trajectories, we generate D^K uncorrelated wiener process, where D is the noise dimension of the given circuit. From D^K total samples, the calculation procedure for the given circuit state variables (current, voltage etc.) is repeated for M Monte-Carlo trails. The hypothesis testing is carried out on those samples generated from M observations. In general, there is no theory that governs the number of trials in Monte-Carlo simulation. However, a trade off exists between the number of trials and the simulation run-times. The higher confidence can be gained by choosing more number of samples, but at the cost of run-times [27].

Algorithm 1 Process Parameter Variation

Require: lower_bound, nominal_bound, upper_bound, randn, inc, sigma_bound, n

Ensure: $n > 0$

1: $Dist \leftarrow lower\_bound : inc : upper\_bound$

2: $PDF \leftarrow (1/(\sqrt{(2 \times \pi)} \times sigma\_bound)) \times exp(\frac{-(Dist-nominal\_bound)^2}{(2\times(sigma\_bound)^2)})$

3: $Param \leftarrow sigma\_bound \times randn(n, 1) + nominal\_bound$

4: **return** $Param$

Figure 2 shows the methodology for Monte-Carlo based on hypothesis testing. The statistical property, is expressed as a null hypothesis H_0 and alternative hypothesis H_1 and is verified if H_0 is accepted, else, the monitor reports the violation of the property. The detailed procedure for Monte Carlo hypothesis testing is illustrated in Algorithm 2, where, T_{obs} is observed value, n is the sample size, σ is the population standard deviation, $\bar{\sigma}$ is the standard error of the sample, μ denotes the population mean, D is the noise dimension, and $SEED$ represents the random seed generation.

Given the number of trajectory $Trac$, based on the simulation step-size (ΔT) and D,

Algorithm 2 SDE based Monte-Carlo Hypothesis Testing

Require: Trac, Param, ΔT
Require: α, T_{obs}, n, σ, $\bar{\sigma}$, μ, $SEED$
Require: $lower, nominal, upper, randn, inc, sigma$
Ensure: $Trac \neq 0$ and $Trac > 0$
Ensure: $Param \neq 0$

while $Trac \neq 0$ **do**
  $W \leftarrow wiener\_process\_generator(\Delta T, SEED)$
  $Param \leftarrow param\_generator(lower, nominal,$
  $upper, randn, inc, sigma, n)$
  $T_{obs} \leftarrow sde\_model(\Delta T, Param, W)$
  for $i = 1$ to M **do**
    $r = random\_number\_generator(n)$
    $s = \sigma \cdot r + \mu$
    $T_{mc}(i) = (mean(s) - \mu)/\bar{\sigma}$
  end for
  while $Upper\ Tail\ Test$ **do**
    $critical\_value = quantile(T_{mc}, 1 - \alpha)$
    if $T_{obs} > critical\_value$ **then**
      $Reject\ H_0$
    else if $T_{obs} < critical\_value$ **then**
      $Accept\ H_0$
    end if
  end while
  while $Lower\ Tail\ Test$ **do**
    $critical\_value = quantile(T_{mc}, \alpha)$
    if $T_{obs} < critical\_value$ **then**
      $Reject\ H_0$
    else if $T_{obs} > critical\_value$ **then**
      $Accept\ H_0$
    end if
  end while
  $Error\_Margin \leftarrow quantile(\frac{1-\alpha}{2}, \sigma, N)$
end while

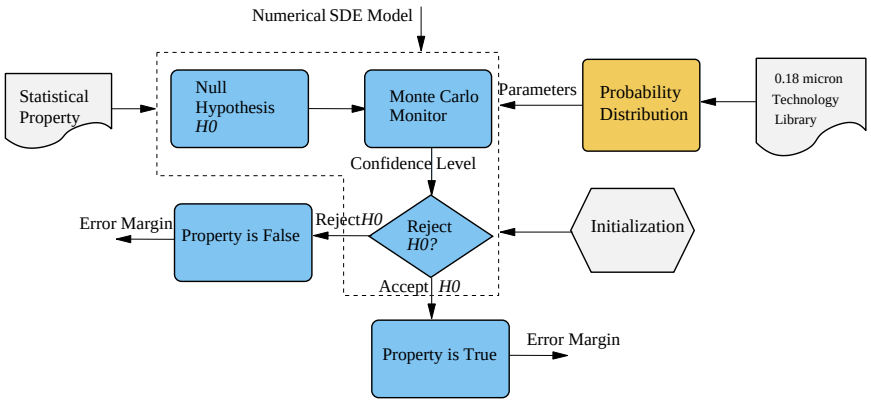


Figure 2: Monte-Carlo Based Hypothesis Testing

we generate D^{Trac} sets of Wiener process and circuit parameters. We then use Monte-Carlo method (line 5) to randomly calculate the desired values. Using the value of the Wiener process and circuit parameters in *sde_model*, we generate the observed value T_{obs} as described in line 7. The loop between line 9 and line 13 is the Monte-Carlo simulation repeated for M trials for hypothesis testing. In each trial, we randomly sample from the distribution of population under the null hypothesis with the same sample size n and then calculate and record the observed value T_{mc} (line 12). For upper tail test, the hypothesis testing is performed afterwards (from line 13 to line 20).

If the observed value T_{obs} is greater than the critical value we reject the null hypothesis H_0. Otherwise, we retain H_0. The *quantile* procedure (line 14) is used to determine the decision about the rejection of a hypothesis [27]. For any simulation technique, it is unlikely that the observed value of the sample is exactly equal to the true value, hence, it is more useful to provide an error margin as shown in line 21.

5 Experimental Results

To illustrate the efficiency of the proposed methodology, we have applied it on several benchmark circuits. The circuit diagram for a MOS transistor based Colpitts oscillator is shown in Figure 3. For the correct choice of component values the circuit will oscillate due to the bias current and negative resistance of the passive tank. The frequency of oscillation is determined by L, C_1 and C_2. For simplicity, we assume the noise only from the passive elements, while the noise from the MOS transistor is ignored.

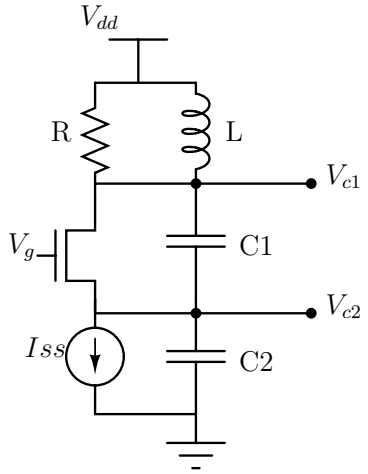


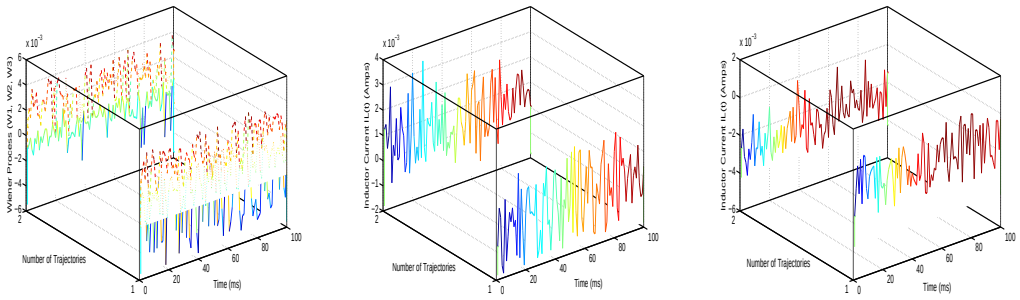
Figure 3: Colpitts Oscillator

5.1 Statistical Property Observations

The deterministic property that was verified [23] is: *whether for the given parameters and initial conditions, the inductor current is within a certain bound or not?* However, for statistical run-time verification one would be interested to know *whether for the given confidence level α, process variation and M Monte Carlo trials, what is the probability of acceptance and rejection of inductor current for multiple trajectories $Trac$?* As a result, the null hypothesis H_0 and the alternative hypothesis H_1 of this property can be expressed as

$$\begin{array}{ll} H_0 & : -0.004 \leq I_L \leq 0.004; \\ H_1 & : I_L > 0.004 \quad or \quad I_L < -0.004; \end{array} \tag{8}$$

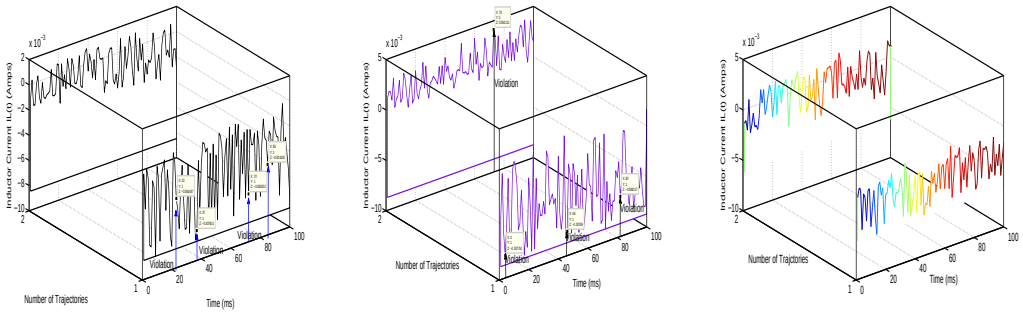
The Monte Carlo experiments were conducted on an ULTRA SPARC-IIIi server (177 MHz CPU, 1GB memory) for the confidence level $\delta = 0.95$ ($\alpha = 0.05$). Since a large value would provide the evidence for the rejection of the null hypothesis H_0, an upper tail test scenario is considered in this case. In order to gain high confidence, we investigated different case studies for analyzing the statistical property of the Colpitts oscillator that are outlined in Table 2. The behavior of the Colpitts oscillator circuit in the presence of noise and process variation is shown in Figure 4 and 5. For simplicity,



(a) Wiener Process W_1, W_2, W_3 (b) *CASE I*: Varying R, C and L (c) *CASE II*: Constant R, L, C

Figure 4: Simulation Result of Colpitts Oscillator.

we show the results of the inductor current for two trajectories only but with multiple violations. Rather than observing the output for each trajectories and reporting any violation, one can achieve certain degree of confidence (say, 95%), by following a statistical approach for the above simulation. This could be based on the acceptance or rejection of null hypothesis H_0 as summarized in Table 2.



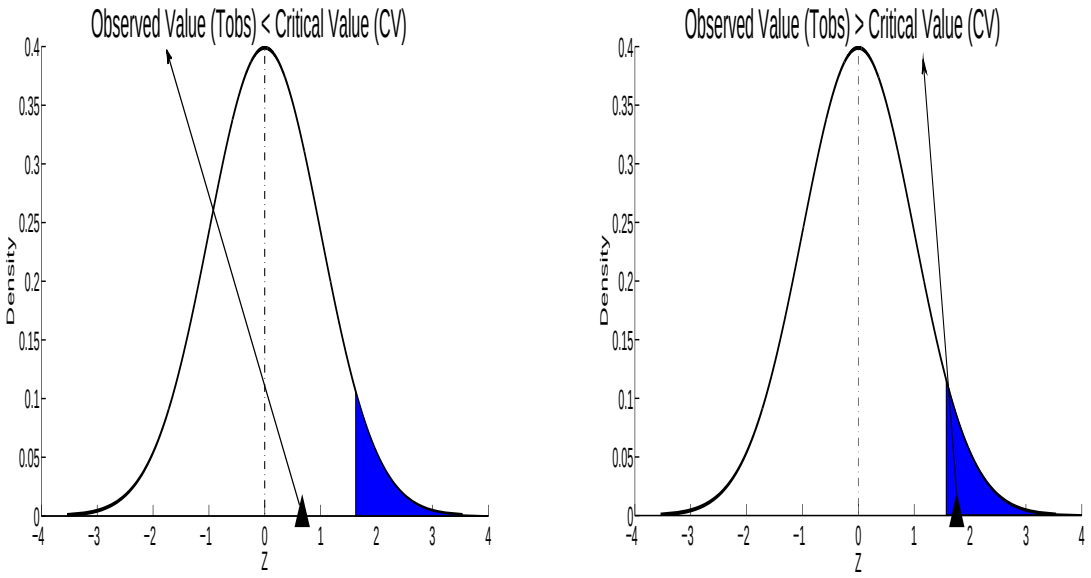
(a) *CASE III*: Constant R and Varying C and L (b) *CASE IV*: Constant C and Varying R and L (c) *CASE V*: Constant L and Varying R, C

Figure 5: Simulation Result of Colpitts Oscillator.

Table 2: Statistical Runtime Verification Results for Colpitts Oscillator.

TRAC = 11, P.V = Process Variation, T = Simulation Time (Sec)												
Monte-Carlo Trials	**Without Noise & P.V**			**With Noise Only**			**With P.V Only**			**With Noise & P.V**		
	Reject	Accept	T	Reject	Accept	T	Reject	Accept	T	Reject	Accept	T
1000	0	11	118	1	10	371	0	11	117	6	5	475
10000	0	11	247	4	7	971	1	10	319	5	6	1263
25000	0	11	316	4	7	2121	1	10	320	7	4	2431
50000	0	11	391	5	6	6173	1	10	420	7	4	7021
100000	0	11	403	7	4	16473	2	9	463	9	2	17021

The acceptance of the null hypothesis H_0 indicates that the property is satisfied and the rejection of H_0 indicates that the property is violated and the current through the inductor (T_{obs}) is larger than the specification (Critical Value) as shown in Figure 6.



(a) Accept Null Hypothesis H_0 (b) Reject Null Hypothesis H_0

Figure 6: Effects of Confidence Level Selection.

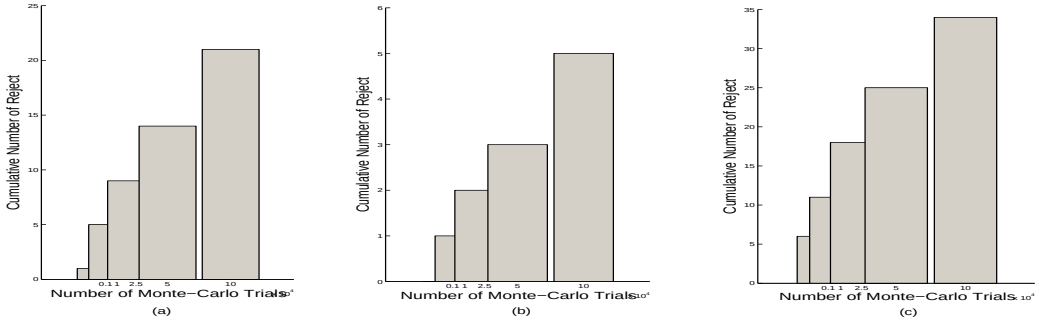


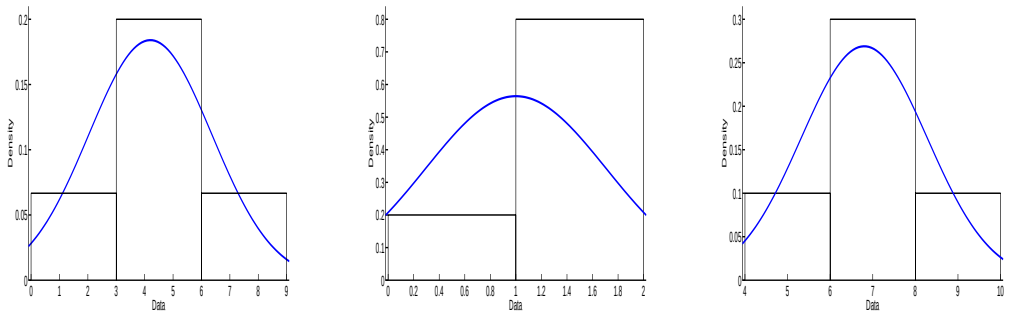
Figure 7: Acceptance/Rejection Cumulative Distribution for Table 2.

From Table 2, we see that for the analysis in the absence of noise and process variation, from columns 2-4, the null hypothesis (H_0) has 100% acceptance mainly because the observed value T_{obs} is less than the critical value $C.V$. However, when we consider the effect of noise only (columns 5-7), based on the number of Monte-Carlo trials, we see more number of rejection of H_0. This is because, the additive Wiener process in the SDE model makes the inductor current to deviate from its specified value. It is also evident from columns 8-10, analysis with parameter variation due to $0.18\mu m$ have shown little failures compared with noise. This is because $\pm 3\sigma$ parameter variation is not large enough to create discrepancy on the inductor current. A more detailed analysis of the process variation is summarized in Table 3. In contrast, in columns 11-13 of Table 2, it is evident that the effect of noise and process variation have led to maximum rejection of the statistical property.

Though we have achieved a good insight on the simulation results, the question is:

Table 3: Effect of Process Variation on Accept/Reject of H_0

TRAC = 11, R = Reject, A = Accept, T = Simulation Time (Sec)									
Monte-Carlo	**Constant R**			**Constant L**			**Constant C_1, C_2**		
Trials	R	A	T	R	A	T	R	A	T
1000	0	11	118	1	10	117	0	11	118
10000	0	1	301	4	7	300	1	10	321
25000	0	11	321	4	7	319	1	10	319
50000	0	11	397	5	6	401	1	10	411
100000	0	11	471	7	4	469	2	9	470



(a) Noise Rejection PDF (b) PV Reject PDF (c) Noise and PV PDF

Figure 8: Reject Probability Density Function Distribution for Table 2.

Does the number of Monte Carlo trials have an impact on the outcome of the hypothesis? We carried out the hypothesis testing for different Monte Carlo trials and the results are summarized in Tables 2 and 3. As seen from both tables, it is apparent that with more number of Monte-Carlo trials, the hypothesis testing will have the leverage to work on a larger group of samples and hence it can provide us with a better assessment of the statistical property, but at the cost of simulation run-times. The best way to describe the results of the statistical property is through cumulative distribution as shown in Figure 7.

The distribution is plotted based on the cumulative sum of the number of acceptance/rejection for the results summarized in Table 2. Figures 4 (a), (b) and (c) represent the distribution for the case of noise only, process variation only and the combined effect of noise and process variation respectively. We see that the rejection gradually increase with the number of Monte-Carlo trials. Also, the number of rejection is dominated by the effect of noise than process variation as seen in Figures 4 (a) and (b). But, it is obvious, that the maximum rejection occurs due to the combined effect of noise and process variation as shown in Figure 4 (c). In summary, the hypothesis test results can be different for different confidence levels and the accuracy would be compromised if the confidence level is too high or too low. The confidence level of 100% is impossible to reach.

6 Conclusion

In this paper, we have presented an approach for noise modeling SDEs, and then integrated the device variation due to the *0.18μm* fabrication process in an SDE based simulation framework for verifying statistical properties of the designs. For illustration purposes, we have used the proposed method to verify the statistical behavior of a Colpitts oscillator circuit.

Our proposed approach is limited to noise in passive elements and we would like to investigate other types of noises. Also, we plan to extend our methodology to handle higher order designs such as phase locked loops (PLL) and verify complex properties that involve the use of second order SDEs. We also need to test the feasibility of other numerical models such as Taylor approximation [18] for accuracy and stability and decide on the appropriate ones for practical applications.

References

[1] *0.18μm* CMOS Fabrication Process. `http://www.tsmc.com`, 2008.

[2] B. Ankele,W. Hölzl, and P. O'Leary. Enhanced MOS parameter extraction and SPICE modeling for mixed signal analogue and Digital Circuit Simulation. IEEE International Conference on Microelectronic Test Structures, pp. 133137, 1989.

[3] B. Oksendal. Stochastic Differential Equations: An Introduction with Applications. Springer, 2000.

[4] Efficient Noise Analysis for Complex Non-Periodic Analog/RF Blocks, Berkeley Design Automation, Inc. 2009

[5] D. Abercrombie, B. Koenemann. Process/Design Learning from Electrical Test. IEEE/ACM International Conference on Computer-Aided Design, pp. 733 - 738, 2004.

[6] D. A. Johns and K. Martin. Analog Integrated Circuit Design, Wiley, 1997.

[7] E. Clarke, A. Donze and A. Legay. Statistical model checking of mixed-analog circuits with an application to a Third-Order delta-sigma modulator. Springer, 2008.

[8] E. Barke, D. Grabowski, H. Graeb, L. Hedrich, S. Heinen, R. Popp, S. Steinhorst and Y. Wang. Formal Approaches to Analog Circuit Verification. Design, Automation and Test in Europe, pp. 724-729, 2009.

[9] $f$reeda^{TM}: `http://www.freeda.org/`, 2009.

[10] E.M. Clarke, O. Grumberg, and D.A. Peled. Model Checking. MIT press, December 1999.

[11] HSPICE User Guide: RF Analysis. `http://www.synopsys.com`, 2009.

[12] M. Bühler, J. Koehl, J. Bickford, J. Hibbeler, R. Sommer, M. Pronath, and A. Ripp. DFM/DFY Design for Manufacturability and Yield - Influence of Process Variations in Digital, Analog and Mixed-Signal Circuit Design. Conference on Design, Automation and Test in Europe, pp. 387 - 392, 2006.

[13] N. M. Kriplani, A. Victor and M. B. Steer. Time-Domain Modelling of Phase Noise in an Oscillator. European Microwave Conference, pp. 514-517, 2006.

[14] O. Maler and D. Nickovic. Monitoring Temporal Properties of Continuous Signals. Formal Modelling and Analysis of Timed Systems, LNCS 3253, 152-166, Springer, 2004.

[15] P. A. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer. Analysis and Design of Analog Integrator Circuits, Wiley, 2009.

[16] P. Antognetti and G. Massobrio. Semiconductor Device Modeling with SPICE, McGraw-Hill, New York, 1988.

[17] P. Bolcato and R. Poujois. A new approach for noise simulation in transient analysis. IEEE International Synposium on Circuits and Systems, pp. 887-890, 1992.

[18] P. E. Kloden and E. Platen. Numerical Solution of Stochastic Differential Equations. Springer, 1995.

[19] P. Paper, M. Jamal Deen and O. Marinov. Noise in Advanced Electronic Devices and Circuits. AIP International Conference on Noise in Physical Systems and 1/f Fluctuations, 780: 3-12, 2005.

[20] R. Narayanan, B. Akbarpour, M. H. Zaki, S. Tahar, and L. Paulson. Formal Verification of Analog/RF Circuits in the Presence of Noise and Process Variation. IEEE/ACM Design, Automation and Test in Europe, pp. 1309-1312, 2010.

[21] R. Narayanan, N. Abbasi, M. Zaki, G. Al Sammane, and S. Tahar. On the Simulation Performance of Contemporary AMS Hardware Description Languages. IEEE International Conference on Microelectronics, pp.390-293, 2008.

[22] R. Narayanan, N. Abbasi, G. Al Sammane, M. Zaki, and S. Tahar. A Comparative Study of AMS Circuit Simulation in VHDL-AMS and SystemC-AMS. International Conference on Embedded Systems & Critical Applications, pp.23-28, 2008.

[23] R. Narayanan, M. Zaki, and S. Tahar. R. Narayanan, M. Zaki, S. Tahar: Using Stochastic Differential Equation for Verification of Noise in Analog/ RF Circuits. Journal of Electronic Testing: Theory and Applications, 26(1): pp. 97-109, Springer, 2010.

[24] R. Narayanan, M. Zaki and S. Tahar. Using Stochastic Differential Equation for Assertion Based Verification of Noise in Analog/RF Circuits. IEEE Mixed-Signals, Sensors, System Test Workshop, pp. 1-8, 2009.

[25] The MathWorks - MATLAB, www.mathworks.com 2008.

[26] T. K. Rawat, A. Lahiri, and A. Gupta. Noise Analysis of Single-Ended Input Differential Amplifier using Stochastic Differential Equation, International Journal of Computer, Information, and Systems Science, and Engineering, 2(3):192-196, 2008.

[27] W. L. Martinez and A. R. Martinez. Computational Statistics Handbook with MATLAB. Chapman & Hall/CRC, 2002.

[28] W. Mathis, and T. Thiessen. On Noise Analysis of Oscillators Based on Statistical Mechanics, International Conference on Mixed Design of Integrated Circuits & Systems, pp. 472-477, 2009.

[29] Y. Cheng. The Influence and Modeling of Process Variation and Device Mismatch on Analog/RF Circuit Design. IEEE International Caracas Conference on Devices, Circuits and Systems, 2002.

[30] Z. Wang, M. H. Zaki, and S. Tahar. Statistical Runtime Verification of Analog and Mixed Signal Designs. In Proc. IEEE International Conference on Signals, Circuits and Systems. pp. 1-6, 2009.