Automated Formal Verification of Analog/RF Circuits in the Presence of Noise

Rajeev Narayanan[1], Behzad Akbarpour[1], Mohamed H. Zaki[2], Sofiène Tahar[1] and Lawrence C. Paulson[3]

[1]Dept. ECE, Concordia University, Montreal, Quebec, Canada Email: {r_naraya, behzad, tahar}@ece.concordia.ca

[2]Dept. CS, University of British Columbia, Vancouver, British Columbia, Canada Email: mzaki@cs.ubc.ca

[3]Computer Laboratory, University of Cambridge, UK Email: lp15@cam.ac.uk

Technical Report

June 6, 2009

Abstract

We model and verify noise in analog/RF designs using an automated theorem prover. We model the designs using stochastic differential equations (SDE), due to the statistical nature of noise. We find a closed form solution for the SDEs based on stochastic calculus, and then verify properties using the MetiTarski theorem prover. Our approach is illustrated on an *RL* High-Pass Filter and a Sample-and-Hold Bottom-Plate Mixer circuit.

Contents

1 Introduction **4**

2 Related Work **4**

3 Preliminaries **5**
3.1 Stochastic Differential Equation 5
3.2 MetiTarski 6

4 Proposed Methodology **7**

5 Applications **7**
5.1 Example 1: RL High-Pass Filter 8
5.2 Example 2: Sample-and-Hold Mixer Circuit 11

6 Conclusion **12**

1 Introduction

In recent years, advanced technologies have allowed designers to develop smaller, faster, low power integrated analog/RF/digital designs in a single chip, known as systems-on-a-chip (SoC). With this complex integration among various blocks and due to nonlinear dynamics of analog/RF designs, effects like inheritance or interactive noise have been responsible for inexplicable design failures [10]. In general, the sources of noise could be due to unwanted interaction between the different circuit blocks (e.g., interference noise) or it could be inherited from the circuit elements (e.g., thermal, shot and flicker) [11]. To fully understand the influence of noise on the overall performance of the analog/RF design and meet the specification, it is necessary to model and verify all the dynamics involved in the design. Hence, a growing number of research groups and industry have looked at the effect of noise during the various design and verification phases.

The first step is to find an adequate model for analog/RF designs with noise. Unfortunately, the usual statistical analysis of stochastic processes does not allow designers to describe the random behavior of a system in the time domain. In fact, for a time-invariant design model, the assumption is that noise does not affect the operating points and the inputs are periodic. However, when the noise is large and the operating points vary due to nonlinearity, accurate results can only be achieved through transient simulation. Due to the statistical behavior of the noise, we are interested in finding a statistical solution rather than a detailed response of the system, therefore we propose to use stochastic differential equations (SDE) [3] as an analog/RF noise model allowing designers to capture the statistical properties of the design in continuous-time. However, the challenge is to incorporate verification techniques that are suited for SDE based modeling.

2 Related Work

For noise analysis, current industrial designs rely heavily on the harmonic-balance method in the frequency-domain and monte-carlo techniques in the time-domain, which of course will still be important in future. The former suffers from capacity problems, while the monte-carlo based technique suffers from expensive simulation run-times. More recently, model checkers such as PRISM [1] have been advocated for formal modeling and analysis of probabilistic systems because of their ability to support different types of probabilistic models. In [6], statistical based model checking has been successfully used to verify saturation property in a simple analog circuits such as a third-order $\Delta\Sigma$ modulator [6]. However, no such model checker has been used to verifying noise in analog circuits. Also, for large circuits model checking can easily run into state-space explosion. To overcome the drawbacks, Akbarpour and Paulson [2] have proposed an automatic proof procedure for inequalities on elementary functions called MetiTarski and which we will adapt in this paper. They have successfully verified control and hybrid systems such as the inverted pendulum and a magnetic disk drive reader system. However, the challenge is to incorporate the above technique for noise verification using

SDEs. There exist a number of efficient SAT solvers that can be considered for automatic checking of inequalities. For example, bounded model checker such as HySAT [8] that combines arithmetic constraints over real- and integer-valued variables can only prove if a property is unsatisfied.

In summary, though there is on-going research that targets analog design modeling and verification, none of them provides a common platform for reasoning about noise in a formal framework. In this paper, we take this verification process a step further, by investigating the usefulness of an automated theorem prover for analog/RF designs, especially in the presence of noise. We propose an SDE based verification methodology in a theorem proving environment using MetiTarski [2]. MetiTarski combines a resolution theorem prover with set of axioms and a decision procedure to automatically prove inequalities concerning the elementary functions such as *sine, cosine, exp.* As most of the closed form solution in an analog/RF circuits involve elementary functions it is intriguing to study the effects of noise using MetiTarski. Our approach is illustrated on a *RL* High-Pass Filter and a Sample-and-Hold Bottom-Plate Mixer circuit.

3 Preliminaries

3.1 Stochastic Differential Equation

A SDE is an ordinary differential equation (ODE) with stochastic process that can model unpredictable real-life behavior of any continuous systems [3]. A stochastic process is a collection of random variables $\{X_t;\ t\ \epsilon\ T\}$ defined on a given probability space indexed by the parameter time t that vary over an index set T. The random term in SDE can be purely additive or it may multiply with some deterministic term [3]. For Example, consider the population growth model describe by the following differential equation

$$\frac{dN}{dt} = a(t)N(t); \quad N(0) = A \tag{1}$$

where *N(t)* is the size of the population at time t, and *a(t)* is the relative rate of growth at time t and A is some initial constant. But, *a(t)* is unknown and is random in nature. Hence a reasonable mathematical interpretation of the randomness for the above equation can be described as

$$\frac{dN}{dt} = a(t)N(t) + \xi_t N(t); \quad N(0) = A \tag{2}$$

The term *a(t)N(t)* is the deterministic drift coefficient while the term $\xi_t N(t)$ represents the stochastic effect [3]. However, in SDE terminology, the above equation can be represented in two forms [3]: *Itô* or *Stratonovich* for more mathematical explanation of *Stratonovich* form. If we consider ξ_t to be the pathwise derivative of Brownian motion (or Wiener Process) dB_t, then Equation 2 can be written in *Itô* differential and integral form as given by

$$\begin{aligned} dN &= a(t)N(t)dt \quad &+N(t)dB_t \\ N &= \int_0^t a(s)N(s)ds \quad &+\int_0^t N(s)dB_s \end{aligned} \tag{3}$$

However, to solve Equation 3 traditional calculus lack the structure to handle stochastic process, and hence we need special mathematical interpretation in the form of stochastic calculus to solve the equations involving brownian motion [3]. A Brownian (or a Wiener process) is a family of random variables W_t, indexed by nonnegative real numbers t, defined on a common probability space with the following properties:

- $W_0 = 0$.
- With probability 1, the function $t \rightarrow W_t$ is continuous in t.
- The process W_t has stationary, independent increments.
- The increment W_{t+s} - W_s has the Normal(0, t) distribution.

In addition, stochastic calculus uses the concept of expectation and *Itô* isometry to solve SDEs. Expectation determines the behavior of any system in the absence of randomness and hence it is easy to conclude that the expectation of any random process (Brownian or Wiener) is zero. As brownian motion cannot be solved using definite integral, the goal of *Itô* isometry is to replace the brownian motion $dB_s$by deterministic term ds for solving SDEs. Table 1 summarizes some of the theorem and axioms that will be adopted in this research for solving SDEs.

Table 1: SDE Formulas [3]

Expectation of a Brownian motion	$\int_0^t F_s dB_s = 0$
Substitution-by-parts	$d(e^t X_t) = e^t X_t dt + e^t dX_t$
Itô Isometry Property	$E\left(\left[\int_0^t F_s dB_s\right]^2\right) = E\left(\left[\int_0^t F_s^2 ds\right]\right)$
Noise	$N_t = X_t - E[X_t]$
Variance of the noise	$Var[N_t^2] = E[X_t^2] - E[X_t]^2$

3.2 MetiTarski

MetiTarski [2] combines a resolution theorem prover with a set of axioms and a decision procedure to automatically prove the elementary functions. As most of the closed form solution in an analog/RF circuits involve elementary functions such as *sine, cosine, exp, log, etc.,* it is intriguing to study the effect of noise using MetiTarski.

In general, MetiTarski turns the verification property into an inequality over special functions and is included as a first-order formula. Since MetiTarski uses polynomial substitution for special functions, axioms must be appended in every format to tell what clauses to be used. For example, to prove that the current in the *RL* High-Pass Filter is less than or equal to certain threshold in MetiTarski, we follow the following syntax

```
fof(RL_Circuit,conjecture, ! [X] :
   (
    (0 ≤ X & X ≤ 0.1) =>0.1*(1−exp(−50*X)) + 0.01*(1−exp(−100*X)) ≤ 0.15)
   ).
```

where "fof" indicates the logic language used is a first-order formula. It is followed by a label name, in this case it is $RL\_Circuit$, and a keyword "$conjecture$" indicating that the following formula is to be proved with the included axioms. The above formula can be read as follows: For All (!) X between 0 to 0.1, the formula which represents the current through the inductor is always less than or equal to *0.15* amps. The first part in the formula $0.1 * (1 - exp(-50 * X))$ is the deterministic value of the current through the inductor, and the second part $0.01 * (1 - exp(-100 * X))$ is the variance of the output current due to noise. The main advantage of the using MetiTarski is that its a complete proof with logical inference steps generated automatically, thereby giving raise to higher confidence in the proof.

4 Proposed Methodology

Figure 1 depicts the proposed SDE based methodology using the automated theorem prover MetiTarski for noise verification in an analog/RF circuit. Thereafter, given an analog/RF design described as a system of *ODEs*, the idea is to include a stochastic process that describes the noise behavior. Since there are no functions/procedures that can automatically incorporate stochastic processes, we manually generate the *SDEs* of the form described in Equation 3. Though, there are some tools that can solve simple SDEs, most of the real-world problems have to be solved manually using theorems shown in Table 1. Subsequently, the environment constraints such as amplitude of noise, initial conditions of the circuit current and voltages are included in the SDEs to get a closed form solution. The closed form solution allows us to express the properties of interest as inequalities over special functions. Since, MetiTarski uses polynomial substitution for special functions, appropriate axioms must be appended to every problem.

If MetiTarski is successful, it delivers a proof and we are done. If unsuccessful, it will run until terminated by the user. Additional axioms are then added or removed in formulating a proof. Including them for special functions that take extreme values will increase the computation time. If still unsuccessful, range reduction is applied to the trigonometric functions to further eliminate any extreme values that can cause problems for MetiTarski's decision procedure. In general, automated methods using MetiTarski develop a complete proof with logical inference steps, thereby providing high confidence in the design.

5 Applications

We have applied the proposed methodology to analog/RF circuits, including a RL High-Pass Filter [7] and a Sample-and-Hold Bottom-Plate Mixer circuit [5]. The experiments

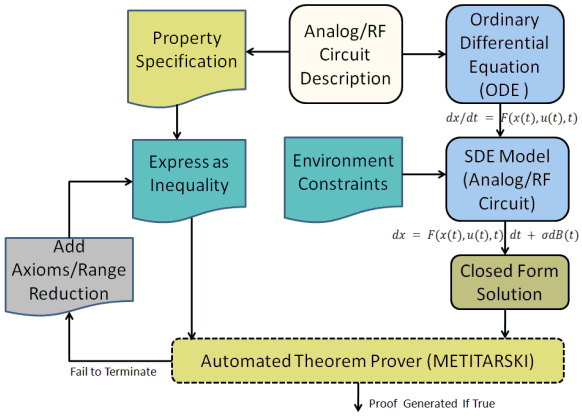

Figure 1: SDE based Verification Methodology using MetiTarski

were all performed on a ULTRA SPARC (177 MHz CPU, 1024 Mbyte memory).

5.1 Example 1: *RL* High-Pass Filter

The circuit diagram of a RL high-pass filter is shown in Figure 2. The filter uses a series resistor R and a shunt inductor L connected to an input source V_{in} to accomplish high-pass filtering.

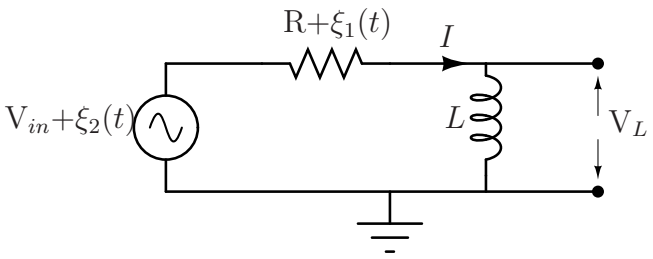

Figure 2: RL High-Pass Filter Circuit [7].

The high-pass filter circuit can be described as

$$L\frac{dI}{dt} + RI(t) = V_{in}(t), \quad I(0) = I_0 \tag{4}$$

Assuming a white noise process at the input voltage source V_{in} and at the resistor R, Equation 4 can be rewritten to incorporate randomness as given by

$$L\frac{dI}{dt} + (R + \alpha\xi_1(t))I(t) = V_{in}(t) + \beta\xi_2(t) \tag{5}$$

where $\xi_1(t)$ and $\xi_2(t)$ are two independent white noise processes, and α and β describe the amplitude of the noise. Equation 5 represents *Itô* SDE in differential form. Replacing ξ_t in Equation (5) by Brownian motion derivative, we get

$$dI_t = \left(-\frac{R}{L}I_t + \frac{1}{L}V_{in}(t)\right)dt + \frac{1}{L}dB_t \tag{6}$$

In the above equation, the first term is the deterministic part, which describes the trajectory of the output process without noise, and the second term is the stochastic part, which modifies the output trajectory due to noise. Our aim is to extract information such as mean $\mathrm{E}[I_t]$ and variance $\mathrm{E}[I_t^2]$, because the mean represents the output trajectory in the absence of noise and variance gives the amount of deviation due to noise. Now, the goal is to find a closed form solution using stochastic calculus and the following gives a detailed analysis of extracting the mean and variance for the *RL* High-Pass filter.

First, we formally multiply both side of Equation (6) by $e^{\frac{R}{L}t}$ and by *substitution-by-parts* we have,

$$d(e^{\frac{R}{L}t}I_t) = \frac{1}{L}e^{\frac{R}{L}t}Vin(t)dt + \frac{1}{L}e^{\frac{R}{L}t}dB_t \tag{7}$$

Integrating equation (7) on both sides and taking expectation, we have

$$\boxed{E[I_t] = e^{\frac{-R}{L}t}I_0 + \frac{1}{L}e^{\frac{-R}{L}t}\int_0^t e^{\frac{R}{L}s}Vin(s)ds} \tag{8}$$

Equation (8) represents the equation describing the mean of the output process, which happens to be exactly the same as the differential equation for the system without noise. To calculate $\mathrm{E}[I_t^2]$ we need to use the interpretation of stochastic calculus. By *Itô* isometry property shown in the Table 1 we can formalize,

$$E\left(\left[\int_0^t e^{\frac{R}{L}s}dB_s\right]^2\right) = E\left(\left[\int_0^t e^{\frac{2R}{L}s}ds\right]\right) = \left(\frac{L}{2R}\left[e^{\frac{2R}{L}t} - 1\right]\right) \tag{9}$$

If we now define the output noise to be $\mathrm{N}_t = \mathrm{I}_t$ - $\mathrm{E}[\mathrm{I}_t]$, then by combining Equation (8) and (9) turns out to be,

$$\boxed{Var(I_t) = E\left([I_t - E\left(I_t\right)]^2\right) = E\left(N_t^2\right) = \frac{1}{2RL}e^{\frac{-2R}{L}t}\left[e^{\frac{2R}{L}t} - 1\right]} \tag{10}$$

Equation (8) and (10) represents the closed form solution of the high-pass filter. Now, the next step is to formalize and verify circuit correctness properties for a given set of parameters and input source.

Property Observations

The properties that we verify in this paper are the steady-state condition and gain for different circuit parameters as shown in Table 2, where $\omega = 2\pi f$ and t is the time.

Property 1: $\forall$ G[$\mathbf{I}_L < 0.11$]

We verify that for the set of parameters shown in Table 2, there is a steady-state current. The behavior in question is stated as the bounded safety property, meaning for the property to be satisfied for time $0.1 \geq X \leq 0.5$, the current through the inductor I_L has to reach a steady-state value *0.11* amps. The first-order formula of the above property is described in MetiTarski syntax as

Table 2: RL High-Pass Filter Parameters

Parameter	**Property 1**	**Property 2**
Resistor (R) Ω	50	100
Inductor (L) H	1.0	100e-3
Peak-to-Peak (A) Volts	Not Applicable	1.0
Frequency(f) Hz	Not Applicable	1000
V_{in} Volts	5.0	Asin(ωt)

```
fof(
RL_Circuit,conjecture, ! [X] :
( (0.01 ≤ X & X ≤ 0.4) =>0.1*(1−exp(−50*X))
  +0.01*(1−exp(−100*X))
  < 0.11)).
```

where 'fof' indicates the logic language used is a first-order formula. It is followed by a label name, in this case it is $RL\_Circuit$, and a keyword "$conjecture$" indicating that the following formula is to be proved with the included axioms. The above formula can be read as follows: For All (!) X between 0.01 to 0.4, the formula which represents the steady-state current through the inductor is always less than *0.11* amps. The first part in the formula $0.1 * (1 - exp(-50 * X))$ is the deterministic value of the current through the inductor, and the second part $0.01 * (1 - exp(-100 * X))$ is the variance of the output current due to noise.

Property 2: $\forall$ G[Gain $\leq$ 0.13]
Equation (8) represents the mean and variance of the output current for an input DC voltage. However, if we apply a sinusoidal input $A\sin(\omega t)$ the variance remains unchanged as it is independent of the input voltage, and the expectation turns out to be

$$\begin{aligned} E[I_t] \;=\; & e^{\frac{-R}{L}t} I_0 + [-\mathrm{e}^{\frac{Rt}{L}}(-\omega L + \; \omega L \mathrm{e}^{\frac{Rt}{L}} \cos(\omega t) \\ & - R\mathrm{e}^{\frac{Rt}{L}} \sin(\omega t))(R^2 + \omega^2 L^2)^{-1}] \end{aligned} \tag{11}$$

The property to be proved is stated as the bounded safety property, meaning for the given set of parameters the gain at the output *Gain* of the filter should be $\leq$ *1.3*. In MetiTarski syntax, this property is described as

```
fof(
RL_Circuit,conjecture, ! [X,S,C] :
((0.002≤ X & X ≤0.01 & S^2 + C^2 = 1) =>
 (0.02468513854*exp(−1000*X)− 0.1551637280*S
 +0.9753148615*C + 10.0*exp(−2000*X))
 ≤ 1.3)).
```

Since the Taylor series approximations for *sine* and *cosine* are extremely inaccurate even a short distance from zero, we have replaced the terms *sin(ωt)* and *cos(ωt)* by

new variables S and C constrained to satisfy $S^2 + C^2 = 1$. This makes the problem more abstract and more general.

5.2 Example 2: Sample-and-Hold Mixer Circuit

Consider the mixer circuit shown in Figure 3. A single switch sampling mixer consists

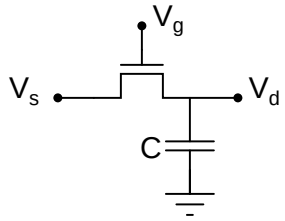

Figure 3: Sample-and-Hold Bottom Plate Mixer Circuit.

of a MOS transistor followed by a sampling capacitor. The input V_s is at RF or IF (Intermediate Frequency). The output V_d is sampled and held on the capacitor when the local oscillator voltage applied at the gate (V_g) goes low. The output is considered in the sampled data domain. This circuit not only serves as a track and hold front end to the A/D conversion but also mixes down RF or IF signals to the baseband. For simplicity, our current analysis is restricted to triode region where the output across the capacitor is given by

$$C\frac{dV_d}{dt} = K(V_{gs} - V_t)V_{ds} - \frac{K}{2}V_{ds}^2 \tag{12}$$

where $K = \mu C_{ox}\frac{W}{L}$, W, L are the width and length of the NMOS transistor, respectively, μ is the electron mobility and C_{ox} is the oxide capacitance. All parameters are technology dependent and assumed to be constant. To avoid harmonic and intermodulation distortion [5], the mixer is designed with small non-linearity. Hence, it is safe to neglect V_{ds}^2. Assuming white noise process ξ_t at the gate input of the transistor, Equation 12 can be rewritten as a *Itô* differential form as

$$g_t X_t dt + K\sigma X_t dW_t + C dX_t = g_t u_t dt + K\sigma u_t dB_t \tag{13}$$

where $V_{gs} = V_g - V_s$ and $V_{ds} = V_d - V_s$; $V_d = X_t$; $g_t = K(V_g - V_t)$; $V_s = u_t$;

Solving for expectation and variance we get

$$\begin{aligned}
E[X_t] &= A(\omega\, C \sin(\omega t) g_t + {g_t}^2(-\mathrm{e}^{-\frac{g_t t}{C}} + \cos(\omega t)))({g_t}^2 + \omega^2 C^2)^{-1} \\
E[N_t^2] &= AQC(\omega^2(-{g_t}^2\mathrm{e}^{-\frac{g_t t}{C}} + S^2C^2\mathrm{e}^{-St} + \cos(\omega\, t)(-S^2C^2 \\
&\quad +{g_t}^2)))({g_t}^2 + \omega^2C^2)^{-1}(SC - g_t)^{-1}(S^2 + \omega^2)^{-1} \\
&\quad +AQC\omega(\sin(\omega\, t)(SC - g_t)(-C\omega^2 + Sg_t) + {g_t}^2S^2(-\mathrm{e}^{-\frac{g_t t}{C}} \\
&\quad +\mathrm{e}^{-St})({g_t}^2 + \omega^2C^2)^{-1}(SC - g_t)^{-1}(S^2 + \omega^2)^{-1})
\end{aligned} \tag{14}$$

Equation (14) represents the mean and variance of the output across the capacitor in the Sample-and-Hold Bottom Plate Mixer circuit. Now we are in a position to formalize and verify correctness properties for the circuit.

Property Observation: $\forall$ **G**$[\mathbf{V}_C \leq \mathbf{0.13}]$
We verify that for a set of circuit parameters shown in Table 3, and within a bounded condition, when the gate voltage V_g is applied, the output across the capacitor V_C is within certain threshold. MetiTarski can prove this property provided it is expressed as

Table 3: Sample-and-Hold Mixer Parameters

Parameter	**Property 1**
V_{th} Volts	0.3
K	50e-6
Peak-to-Peak (A) Volts	0.5
Capacitor (C) F	0.4e-12
Frequency(f) Hz	200e6
V_g Volts	2.5
V_s Volts	Acos(ωt)

```
fof(
Mixer,conjecture, ![X,S,C,SB,CB]:
((0 ≤ X & X ≤10^−7 & S^2 + C^2=1 & SB^2 + CB^2=1) =>

 0.023*C+ 0.104*S − 0.023*exp(−2.75*10^8*X)+ 0.003 +
 0.39*10^−3*CB + 0.52*10^−3*SB +7330*exp(−5.5*10^8*X)

 *X −0.35*10^−2*exp(−5.5*10^8*X)+0.1*10^−3*exp(−2.75
 *10^8*X)*C +0.22*10^−3*exp(−2.75*10^8*X)*S
 ≤ 0.13)).
```

In summary, by turning the verification property into an inequality over special functions, MetiTarski is able to prove the property of interest in the presence of noise for the high-pass filter and sample-and-hold bottom plate mixer circuits. As it is a proof based analysis, this process is much more reliable than manual (visual or textual) inspection of simulation traces which does not guarantee the correctness of the design. Table 4 summarizes the runtime taken by MetiTarski to prove the properties.

6 Conclusion

In this paper, we have presented a practical automated theorem proving verification methodology for noise in analog/RF designs. The approach is based on modeling the

Table 4: MetiTarski Run-Times for Example 1 & 2 (in Seconds)

Circuit	**Run-Times**	
Example 1	Property 1	0.36
	Property 2	81.58
Example 2	22.53	

noise using SDEs and proving properties using MetiTarski. We have used the methodology to verify the steady-state condition and gain of a *RL* High-Pass filter and output behavior of a Sample-and-Hold Bottom-Plate Mixer circuit. The main advantage of the methodology proposed is that its a complete proof with logical inference steps that can even be inspected manually thereby providing confidence during the design development.

Future Work

- Scalability of the proposed methodology has to be investigated, meaning, how the proposed methodology could be used to do noise verification for higher order designs such as $\Delta\Sigma$ modulator and complex circuits like phase locked loops (PLL) with one-dimensional and multi-dimensional noise. This involves solving higher order SDEs using stochastic calculus.

- Not all analog/RF designs have closed form solution, hence there is a need to investigate if Metitarski can prove properties on the numerical approximations that may involve error analysis.

- Current methodology involves rigorous paper-pencil technique, meaning, extracting the SDEs from the ODEs is done manually. One goal is to automate this process.

References

[1] A. Hinton, M. Kwiatkowska, G. Norman and D. Parker. PRISM: A Tool for Automatic Verification of Probabilistic Systems. In Tools and Algorithms for the Construction and Analysis of Systems, LNCS 3920, pages 441-444, Springer-Verlag, 2006.

[2] B. Akbarpour and L. Paulson. Metitarski: An Automatic Prover for the Elementary Functions. In Intelligent Computer Mathematics, LNCS 5144, pages 217-231. Springer-Verlag, 2008.

[3] B. Oksendal. Stochastic Differential Equations. An Introduction with Applications. Springer-Verlag, 2000.

[4] B. Poizat, D. Brandar, and M. Klein, Course of Models Theory. Springer-Verlag, 2006.

[5] D. Ham and A. Hajimiri. Complete Noise Analysis for CMOS Switching Mixers Via Stochastic Differential Equations. IEEE Custom Integrated Circuits Conference, pages. 439-442, 2000.

[6] E. Clarke, A. Donze and A. Legay, Statistical Model Checking of Mixed-Analog Circuits with an application to a Third-Order Delta-Sigma Modulator. Haifa Verification Conference, LNCS 5394, pages 149-163, Springer-Verlag, 2008.

[7] E. Kolarova. Modelling RL Electrical Circuits by Stochastic Diferential Equations. International Conference on Computer as a Tool, pages 1236-1238, 2005.

[8] M. Franzle, C. Herde, T. Teige, S. Ratschan, and T. Schubert. Efficient Solving of Large Non-linear Arithmetic Constraint Systems with Complex Boolean Structure, In Journal on Satisfiability, Boolean Modeling and Computation, Vol 1: pages. 209-236, 2007.

[9] P. Bolcato and R. Poujois. A New Approach for Noise Simulation in Transient Analysis. IEEE International Synposium on Circuits and Systems, pages. 887-890, 1992.

[10] P. Paper, M. J. Deen and O. Marinov. Noise in Advanced Electronic Devices and Circuits. AIP International Conference on Noise in Physical Systems and 1/f Fluctuations, AIP Conference Proceedings, Vol. 780, pages 3-12, 2005.

[11] R. Ludwig and P. Bretchko. RF Circuit Design, Theory and Applications. Pearson Education, 2004.