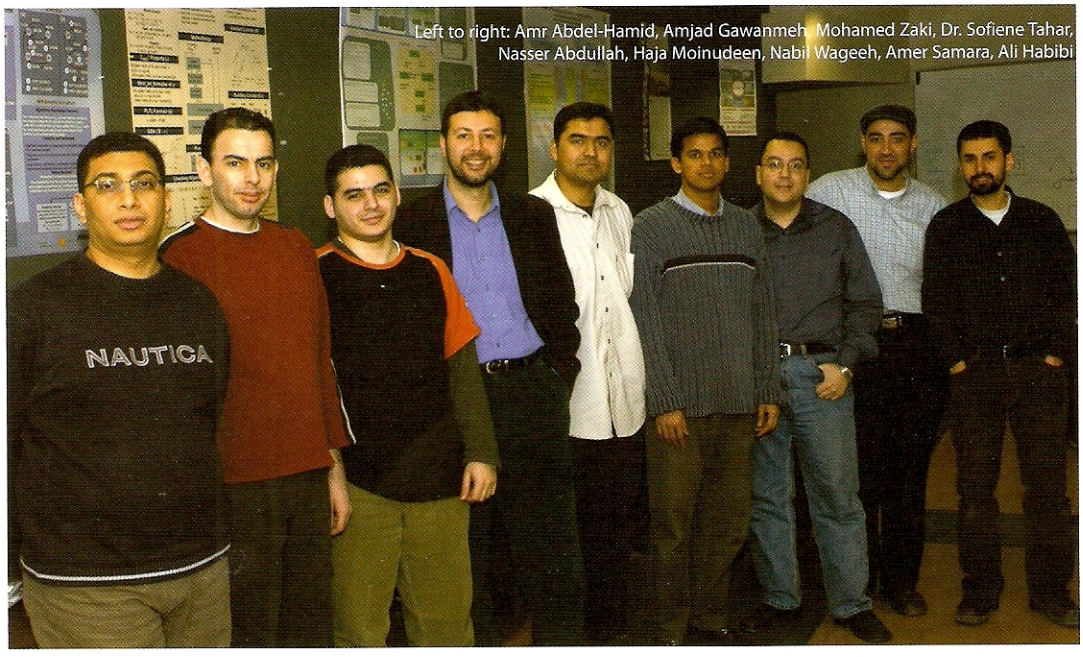
HVG - ECE's Electronic Dream Team

By Shelagh McNally



Left to right: Amr Abdel-Hamid, Amjad Gawanmeh, Mohamed Zaki, Dr. Sofiene Tahar, Nasser Abdullah, Haja Moinudeen, Nabil Wageeh, Amer Samara, Ali Habibi

Faster, smarter, cheaper and sooner. That's what we want from our electronics and this has created a bit of a crisis in the electronics industry. Technology is developing rapidly and holds great promise. But there is one problem; lots of products look good on paper but don't deliver once they are built. The main problem is a lack of standard verification method for functionality. There just isn't one quick and easy way to see if all the components of voice, visuals and text will work together in a certain product. According to Brian Bailey of Mentor Graphics, 60% of all new products fail when it comes to functional verification, even though most companies spend a large portion of their resources on the process. A downturn in the industry economy, plus the need to shorten product cycles, has created enormous pressure to get it right the first time around. But when you have different systems such as analog/mixed signals, microprocessors, embedded memory, signal processing, networking and sensors all combined into one environment, verification becomes a tricky business. This is where Concordia's Hardware Verification Group (HVG) from the Department of Electrical and Computer Engineering comes in, and how they are about to play a crucial role.

Gordon Moore was right. In 1965, Moore made the observation that we would see an exponential growth in the number of transistors per integrated circuit. His prediction became Moore's Law and has proven to be quite accurate. We now have microelectronics with embedded systems that integrate processors, memory, signal processing, networking, and sensors, all on a single chip known as System-on-Chip (SoC). There is no doubt that SoC has changed classical design technology - ten million gates integrated on a single chip will do that. But the industry is now looking at integrating a billion transistors on a single chip in order to get the kind of sophisticated all-in-one technology we all want.

There is some discussion on how these billion transistors will get to that single chip. Some believe it will take the form of a single processor with increasingly sophisticated hardware hidden from the programmer. Others believe that we will see more of the System-on-Chip (SoC) morph into the Multiprocessor SoC (MPSoC) along with an increased use of the Network-on-Chip. These out-of-box systems combining analog and digital are certainly attractive but the same equation remains — the more complex the system, the more likely there will be bugs and problems. So whichever way the billion transistors are added, the principal challenge of verification doesn't really change - in fact, it gets more difficult to do.

The urgency for verification has become an issue within the industry because of market pressure to deliver products quickly. In the EDA game, whoever has the first product on the shelf wins the race. (They are, however, quickly disqualified if the product doesn't work.) Market pressure has seen the turn-around time from developing a paper idea into a prototype shrink to a mere 18 months. That's not a lot of time to get the bugs ironed out of a sophisticated product, particularly when you are required to check each component separately, not knowing if they will continue working once placed alongside the other. But as the industry moves towards these new heterogeneous parallel SoCs, the functional verification gap has actually widened to critical proportions instead of becoming more streamlined to fit the tighter deadlines.

Verification, of course, is what HVG is all about, but they are about to take it to a higher level with their new research project. The group has recently received 25% of a Strategic Research Grant worth $1.4M ($630K cash and $738K in-kind) from the Natural Sciences and Engineering Research Council of Canada (NSERC). This new research project reunites Concordia's **Dr. Sofiène Tahar** with fellow colleagues **Dr. E.M. Aboulhamind** from *l'Université de Montréal*, and **Drs. G. Bois** and **G. Nicolescu** from *l'École Polytechnique*. Competition for this grant was fierce and the team beat out 400 other applicants. Their track record was a principal factor in getting this grant, given other successful past collaborations. "It helped that we had worked on other (strategic) projects together since our strengths and backgrounds really complement each other," explained Dr. Tahar. "NSERC took that into consideration when looking at our proposal."

The Concordia research team will consist of two postdoctoral fellows, eight PhD students and five master students who will be using all available tools to solve the EDA verification problem. Actually, the solution is quite simple (on paper, that is). Find a common language that speaks to both the software and hardware in electronic products. That type of language is commonly referred to as a System Level Language (SLL) and the most reliable SLL for SoC is SystemC. While it is becoming an industry standard, it still lacks strong verification tools and techniques. Unfortunately, those working in the industry are not familiar enough with the language to develop the tools, nor do they have the time. However, Dr. Tahar's group already speaks SystemC and they do have the time. One of their principal innovations was to take the SystemC code and convert it into the Abstract State Machine (ASM) language that can then be checked and tested with a powerful Microsoft Research tool. In other words, they translated the language so that the hardware/software distinction would be removed. Once that barrier is gone, verification can become a one-step procedure. It was a creative way of looking at the problem and surprised many in both the hardware and software industry.

The project is going to continue using SystemC, but will also look at other solutions. Typically, HVG uses four methods of verification: simulation, model checking, assertion-based verification and theorem proving. For now, the group will be using actual prototypes and start off by learning as much as they can about how analog and optical devices work together. By using case studies, examining the actual chips right from the glue logic up to the processing, and engaging in on-site discussions with the engineers, they plan to develop new theories. It's valuable experience for the students because they are getting hands-on training in an area where there is much demand. Dr. Tahar believes that the mix of the practical from the engineering side with the theoretical from computer science is what makes HVG so innovative and poised to solve the verification process. But what makes him the happiest is seeing his graduating students being quickly hired by industry.

The industry is keeping a close eye on the outcome of this project since it may very well be a crucial element in designing the technology of tomorrow. NSERC believes the outcome of the project will impact the Canadian economy, society and the environment within 10 years. Three electronic companies, ST Microelectronics (Canada), Mentor Graphics (US) and Amirix (Canada), are involved in the project, providing a total of $773K in support. "The EDA is desperate for a solution to the problem and has begun to recognize the need for developing the software to build the hardware. They know that this is the place where there are new ideas, new papers and new conferences, without the usual market pressure," explains Dr. Tahar.

HVG is currently negotiating two concrete projects with Cadence and Synopsys, the two biggest players in the EDA industry. For the last few years, it has also maintained strong collaborative research links with Microsoft and Intel. In June 2004, HVG was invited to present their SoC verification project at an industrial forum during the largest EDA Design Automation Conference (DAC) in San Diego, California. Their project on SystemC was selected with five others from 60 submissions. In March 2005, HVG was invited to Munich for the Electronic Design, Automation and Test (DATE) Conference where out of 825 submissions, they were asked to present three papers. DATE only accepts 20% of all papers submitted, and being allowed three papers is not only indicative of the level of interest, but also the calibre of the research. HVG has also become the official host and manager of the North American SystemC User Group's (NASCUG) website at www.nasguc.org/ and for the second consecutive year, HVG is co-organizing the annual NASCUG symposium at DAC being held this June in Anaheim, California.

HVG may just be the team to deliver that promise of faster, smarter and cheaper electronics for the 21st century. For more information on HVG, visit their website at http://hvg.ece.concordia.ca.