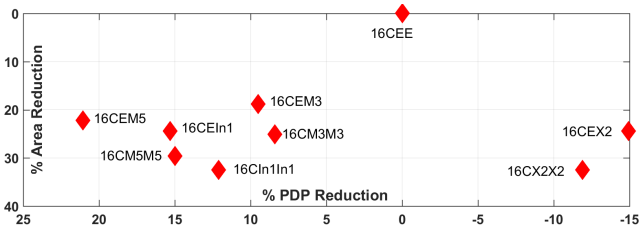

Figure 6: Area and PDP Reduction of 16x16 Tree Multiplier

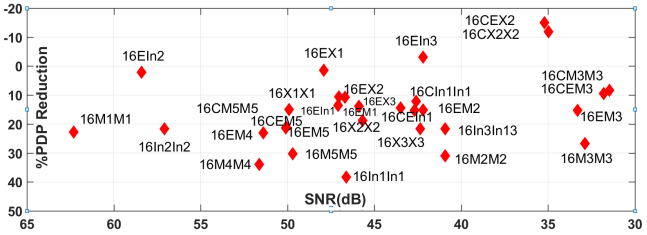

Figure 7: %PDP Reduction and SNR of Multipliers

5.3 Discussion and Comparison

The considered approximate multipliers are implemented using Cadence's Spectre based on TSMC65nm process, with V_{dd} = 1.0V at T=27C°. The circuit inputs are provided by independent voltage sources, and a load of 10fF is utilized. We evaluated and compared the design characteristics (Area, Power and Delay). We found out that the 8x8 exact tree multiplier exhibits lower delay, power and size compared to the 8x8 exact array multiplier.

Several multiplier designs, based on *AMA5*, have the lowest delay and power consumption, due to the basic structure of the FA cell, which is composed of two buffers only. Also, they have the lowest NMED and a small size. Regarding accuracy, the designs based on *InXA1* have low ER and NMED. Similarly, the designs based on the 6 transistors FA, have the minimal size. Thus, it can be observed that the characteristics of approximate FA are generally propagated in the corresponding approximate multipliers as well.

In terms of architecture, we found out that the tree multiplier designs tend to have a lower power consumption than the array multipliers, especially the designs based on low power consumption FAs, such as *AMA3* and *AMA5*. In terms of the 8x8 sub-module placement to form higher-order multipliers, with a fixed configuration for AHxBH, AHxBL and ALxBH, we have noticed that the quality-loss increases, while the size, power consumption and delay decrease for designs with fully approximate ALxBL.

Compared to the 24 different designs reported in [7], where 92% of the designs have ER close to 100%, only 80% of our proposed designs have high ER. Regarding NMED, almost all our designs have a value less than 10^{-5}, which is the minimum value reported by the 24 approximate designs in [7]. Comparing the PDP reduction, most of the designs in [7] have a high PDP reduction because they are based on truncation and a high degree of approximation. However, our designs are superior in PDP reduction for designs with a high degree of approximation.

6 APPLICATION

We evaluate and compare the accuracy of the built approximate multipliers based on an image blending application, where two images are multiplied pixel-by-pixel. While in previous sections, we used Cadence Spectre to build the circuits and evaluate their area, performance and power consumption, for experimentation purposes, here we use MATLAB to evaluate error metrics for an image processing application. The library of implemented cells and multiplier circuits, and the results of the image blending application can be found at *https://sourceforge.net/projects/approximatemultiplier*. The signal to noise ratio (SNR) is used to measure the image quality for different designs. Figure 7 shows a comparison of the SNR and the percentage of PDP reduction for different approximate multipliers. Clearly, designs on the bottom left corner, have the highest PDP reduction and the best quality (high SNR) [8]. Generally, all multiplier designs have an acceptable SNR (acceptable quality).

7 CONCLUSIONS

In this paper, we designed, evaluated and compared approximate multipliers, based on approximation in partial product summation. The design space of approximate multipliers is found to be primarily dependent on the type of the approximate FA used, the architecture, and the placement of 8x8 sub-modules in the higher-order nxn multipliers. The proposed designs are compared based on PDP, area, delay, power, ER and NMED. Various optimal designs have been identified in terms of the considered design metrics. An image blending application is used to compare the proposed multiplier designs in terms of SNR and PDP. Our designs show comparative results compared to 24 different approximate designs reported in [7]. In the future, we plan to investigate the design space of higher-order multiplier modules (e.g., 64x64) using the already considered metrics and configurations. Moreover, we also plan to evaluate the possibility of having mixed FAs in the 8x8 multiplier block.

REFERENCES

[1] J. Han and M. Orshansky, "Approximate computing: An emerging paradigm for energy-efficient design," in *IEEE ETS*, 2013, pp. 1–6.
[2] P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an underdesigned multiplier architecture," in *IEEE VLSI Design*, 2011, pp. 346–351.
[3] H. Jiang, J. Han, and F. Lombardi, "A comparative review and evaluation of approximate adders," in *ACM GLSVLSI*, 2015, pp. 343–348.
[4] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 1, pp. 124–137, 2013.
[5] Z. Yang, A. Jain, J. Liang, J. Han, and F. Lombardi, "Approximate xor/xnor-based adders for inexact computing," in *IEEE Nanotechnology*, 2013, pp. 690–693.
[6] H. A. F. Almurib, T. N. Kumar, and F. Lombardi, "Inexact designs for approximate low power addition by cell replacement," in *IEEE DATE*, 2016, pp. 660–665.
[7] H. Jiang, C. Liu, N. Maheshwari, F. Lombardi, and J. Han, "A comparative evaluation of approximate multipliers," in *IEEE Nanoscale Architectures*, 2016, pp. 191–196.
[8] M. Masadeh, O. Hasan, and S. Tahar, *Comparative Study of Approximate Multipliers*, Technical Report, ECE Department, Concordia University, Montreal, QC, Canada. http://arxiv.org/abs/1803.06587, 2018.
[9] Z. Yang, J. Yang, K. Xing, and G. Yang, "Approximate compressor based multiplier design methodology for error-resilient digital signal processing," in *IEEE ICSIP*, 2016, pp. 740–744.
[10] S. Rehman, W. El-Harouni, M. Shafique, A. Kumar, and J. Henkel, "Architectural-space exploration of approximate multipliers," in *ACM DAC*, 2016, pp. 1–8.
[11] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and analysis of approximate compressors for multiplication," *IEEE Transactions on Computers*, vol. 64, no. 4, pp. 984–994, 2015.
[12] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*. Prentice-Hall, 2002.