# **Comparative Study of Approximate Multipliers**

Mahmoud Masadeh<sup>1</sup>, Osman Hasan<sup>1,2</sup>, and Sofiène Tahar<sup>1</sup>

<sup>1</sup>Department of Electrical and Computer Engineering, Concordia University, Montréal, Canada {m\_masa,o\_hasan,tahar}@ecce.concordia.ca

<sup>2</sup>School of Electrical Engineering and Computer Science, National University of Science and Technology, Islamabad, Pakistan

#### TECHNICAL REPORT

March 2018

#### Abstract

Approximate multipliers are widely being advocated for energy-efficient computing in applications that exhibit an inherent tolerance to inaccuracy. However, the inclusion of accuracy as a key design parameter, besides the performance, area and power, makes the identification of the most suitable approximate multiplier quite challenging. In this paper, we identify three major decision making factors for the selection of an approximate multipliers circuit: (1) the type of approximate full adder (FA) used to construct the multiplier, (2) the architecture, i.e., array or tree, of the multiplier and (3) the placement of sub-modules of approximate and exact multipliers in the main multiplier module. Based on these factors, we explored the design space for circuit level implementations of approximate multipliers. We used circuit level implementations of some of the most widely used approximate full adders, i.e., approximate mirror adders, XOR/XNOR based approximate full adders and Inexact adder cell. These FA cells are then used to develop circuits for the approximate high order compressors as building blocks for 8x8 array and tree multipliers. We then develop various implementations of higher bit multipliers by using a combination of exact and inaccurate 8x8 multiplier cells. All these implementations have been done using the Cadence's Spectre tool with the TSMC65nm technology. The design space of these multipliers is explored based on their power, area, delay and error and the best approximate multiplier designs are identified. The report also presents the validation of our results using an image blending application. An open source library of implemented cells and multiplier circuits are available online.

**Keywords**— Approximate Computing, Approximate Multiplier, Power-Efficiency, Error Metrics, Circuit Characteristics, Comparative Study

# Contents

1	Introduction	4
<b>2</b>	Proposed Methodology	5
3	Approximate FAs and Compressors	7
4	Multiplier Basic Blocks	10
	4.1 8x8 Array Multiplier	10
	4.2 8x8 Tree Multiplier	13
<b>5</b>	Higher-Order Multiplier Configuration	14
	5.1 <b>16x16 Array Multiplier</b>	15
	5.2 <b>16x16 Tree Multiplier</b>	17
	5.3 Discussion and Comparison	17
6	Application	19
7	Conclusions	20

### 1 Introduction

The pervasive, portable, embedded and mobile nature of present age computing systems has led to an increasing demand for ultra low power consumption, small footprint, and high performance. Approximate computing [1] is a nascent computing paradigm that allows us to achieve these objectives by compromising the arithmetic accuracy. Many systems used in domains, like multimedia and big data analysis, exhibit an inherent tolerance to a certain level of inaccuracies in computation, and thus can benefit from approximate computing.

Functional approximation [2], in hardware, mostly deals with the design of approximate arithmetic units, such as adders and multipliers, at different abstraction levels, i.e., transistor, gate, RTL (Register Transfer Level) and application. Some notable approximate adders include *speculative adders* [3], *segmented adders* [4], *carry select adders* [5] and *approximate full adders* [6]. The transistor level approximation provides the highest flexibility due to the ability to tweak most of the design parameters at this level. Various approximate full adders (FA) at the transistor level have been proposed including the mirror adders [7], the XOR/XNOR based FA [8] and the inexact FA [9]. On the other hand, most of approximate multipliers have been designed at higher levels of abstraction, i.e., gate, RTL and application.

Approximate multipliers have been mainly designed using three techniques, i) Approximation in partial products generation: e.g., Kulkarni et al. [2] proposed an approximate 2x2 binary multiplier at the gate level by changing a single entry in the Karnaugh-map with an error rate of 1/16. ii) Approximation in partial product tree: e.g., Error Tolerant Multipliers (ETM) [10] divide the input operands in two parts, i.e., the multiplication part for the MSBs and the non-multiplication part for the LSBs, and thus omitting the generation of some partial products [11]. iii) Approximation in partial products summation: Approximate FA cells are used to form an array multiplier, e.g., in [12] the approximate mirror adder has been used to develop a multiplier. Similarly, Momeni et al. [13] proposed an approximate compressor for building approximate multipliers, but this multiplier is known to give a non-zero result for zero inputs. Jiang et al. [14] compared the characteristics of different approximate multipliers, implemented in VHDL based on the three different techniques mentioned previously. In this work, we target approximate multipliers based on approximation in partial products summation.

In this report, we compare the accuracy and circuit characteristics of different approximate multipliers. These multipliers are designed based on three identified decisions: (1) the type of approximate FA used to construct the multiplier, (2) the architecture of the multiplier, and (3) the placement of sub-modules of approximate and exact multipliers in the target multiplier module. We were able to design approximate multipliers, which are suitable to applications with intrinsic error resiliency. We used these designs in an image processing application and obtained promising results, thus we believe they are applicable in other domains. The rest of the report is organized as follows: The proposed methodology of designing and evaluating approximate multipliers is explained in Section 2. Section 3 explains the design characteristics of approximate FAs and compressors. Section 4 describes different configurations of approximate sub-modules, with different architectures. Target approximate multiplies are designed and evaluated in Section 5. The application of image processing is given in Section 6. Finally, conclusions are drawn in Section 7.

# 2 Proposed Methodology

The design space for approximate multipliers based on different approximate FAs and compressors is quite huge. However, it is difficult to select the most suitable design for a specific application. Figure 1 presents an overview of our proposed methodology to build different approximate multipliers and compare their design metrics to select the most suitable design. It consists of the following steps:

- 1. Building a library of elementary approximate FAs using the TSMC65nm technology in Cadence Spectre: We use the default transistors of this technology to build 11 approximate FA designs comprising of 5 mirror FAs, 3 XOR/XNOR gate FAs and 3 inexact FAs. To the best of our knowledge, these 11 designs are the only ones that exist in the literature at the transistor level.
- 2. *Characterization and early space reduction*: We perform area, power, latency and quality characterizations of different approximate FAs to filter out non-Pareto designs.



Figure 1: Methodology Overview

- 3. Building a library of approximate compressors: We build a Cadence library of approximate compressors using the optimal approximate FA, as recommended by [7].
- 4. Building approximate multipliers basic blocks: Based on approximate FAs and compressors, we design various approximate 8x8 array and tree multipliers, respectively. These proposed designs are related to the ripple-carry array multiplier architecture, which is the most power efficient amonge conventional architectures [15].
- 5. Design target approximate multipliers: Based on different configurations of 8x8 approximate multipliers, the target multiplier modules are designed and characterized.
- 6. *Selection of design points*: Considering the required quality constrains of a specific application, a subset of power-efficient design points is selected.

In order to evaluate the efficiency of the proposed approximate designs, *power* consumption and area, represented by the number of transistors used, are measured, and the circuit performance is measured by the maximum *delay* between changing the inputs and observing the output(s). Besides these basic design metrics, *accuracy* is also an important design constraint in approximate computing. There exist several *error metrics* used in approximate computing to quantify errors and measure accuracy [9], including:

- Error Rate (ER): The percentage of erroneous outputs among all outputs.
- Error Distance (ED): The arithmetic difference between the exact and approximate result.
- Mean Error Distance (MED): The average of EDs for a set of outputs obtained by applying a set of inputs.
- Relative Error Distance (RED): The ratio of ED to exact result.
- Mean Relative Error Distance (MRED): The average value of all possible relative error distances (RED).
- Normalized Mean Error Distance (NMED): The normalization of mean error distance (MED) by the maximum output of the accurate design. This metric is used for comparing circuits (adders and multipliers) of different sizes.

For the evaluation of the accuracy of the approximate FAs, we use the number of erroneous outputs. In the proposed methodology, we evaluate ER, MED, NMED and MRED for the proposed designs. As shown in Figure 1, *the characterization and selection* process is applied at multiple steps to different components, during the design flow. Characterization aims to find the design characteristics of the circuits including area, power consumption, performance, error metrics, and other derived metrics

such as Power-Delay-Product (PDP). The design selection process for the evaluated approximate designs also depends on the application domain of the given circuit. As the design requirements vary from one application to another, our designs are unique because they can provide some degree of error in the output as well and thus this aspect also needs to be covered in the characterization and selection process.

# **3** Approximate FAs and Compressors

Approximate n-bit binary adders can be designed by modifying the carry generation and propagation of the addition process by using several overlapping sub-adders to reduce latency. Some examples include speculative [3], segmented [4] and carry select adders [5]. However, these designs involve several overlapping sub-adders, which makes them unsuitable to build energy efficient circuits. Low power approximate binary adders are generally constructed by replacing the accurate FAs with approximate FAs. We consider five approximate mirror adders (AMA1, AMA2, AMA3, AMA4 and AMA5) [7], three approximate XOR/XNOR based full adders (AXA1, AXA2 and AXA3) [8] and three inexact adder cells (InXA1, InXA2 and InXA3) [9].

Table 1 shows the truth tables of the 11 considered approximate FAs, and their characteristics including Size (A), Power consumption (P), Delay (D), number of Erroneous outputs (E), which indicates the likelihood of at least one output (Cout or Sum) being wrong, and PDP. All approximate FAs are Pareto-points, i.e., they provide less area and power consumption compared to the exact design at the cost of compromising accuracy [16]. Some of the FA designs have an enhanced performance (reduced delay), while other designs have degraded performance due to the internal structure and node capacitance. In [17], AMA5 is considered as a *wire* with zero area and zero power consumption. However, this is unrealistic as the output of AMA5 has to drive other signals. Thus, we used two buffers instead of two wires to design it.

Table 1: Truth Tables of Different Approximate FAs and Comparison of their Characteristics

	Inputs	Exact	FA (E)	AMA	1 (M1)	AMA	2 (M2)	AMA	3 (M3)	AMA	4 (M4)	AMA	5 (M4)	AXA	1 (X1)	AXA	2 (X2)	AXA	3 (X3)	InXA	1 (In1)	InXA	2 (In2)	InXA	3 (In3)
AI	Cin	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout	Sum	Cout
0 0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
0 0	1	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	1	1	0	1	0
0 1	0	1	0	0	1	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	1	0	1	0
0 1	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	0	1	0	1	0	1	1	1	0	1
1 (	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	0
1 (	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	1	0	1	0	1	1	1	0	1
1 1	0	0	1	0	1	0	1	0	1	0	1	1	1	0	1	1	1	0	1	0	0	0	1	0	1
1 1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
	Size		28		20	1	.4	[ :	11	1	15		8		8		6		8		6		8		6
Pe	wer (nw)	70	63.3	6	12	56	1.1	55	58.1	58	7.1	41	12.1	67	6.2	35	8.7	39	6.5	4	10	35	5.1	6	48
D	elay (ps)	1 2	244	1	.95	3	66	3	60	1	96	1	.50	11	155	8	38	14	167	7	'40	8	32	7	67
# of	Error Cases		0		2		2		3		3		4		4		4		2		2	l	2		2
I	DP (fJ)	18	6.25	11	9.34	205	5.36	20	0.92	113	5.07	61	1.82	7	81	30	0.59	5	82	30	03.4	29	5.44	75	3.5

Figure 2 shows the power consumption and delay of individual approximate FAs, where all FAs exhibit a reduced power consumption. But, only the mirror adder based FAs have a reduced delay due to their internal structure. InXA2 and AXA2 have the minimal power consumption with 53% reduction compared to the exact mirror adder (MA). Also, InXA1 and AXA3 have close-to-minimal power consumption. Since



Figure 2: Power Consumption and Delay of Approximate FAs



30 25 20 15 10 5 ο Exact FA AMA1 AMA2 АМАЗ AMA4 AMA5 AXA1 AXA2 АХАЗ InXA1 InXA2 InXA3 Size ER

Figure 3: Power-Delay-Product of Approximate FAs

Figure 4: Size and Number of erroneous outputs (ER) of Approximate FAs

AMA5 is composed of only two buffers, it has the lowest delay while AXA3 has the highest delay due to the threshold voltage drop of the pass transistors. AMA1 and AMA4 both have a close-to-minimal delay. PDP which is a figure of merit correlated with the energy efficiency of a digital design, is shown in Figure 3 for the FAs. Mirror adder based designs have a low PDP values. AMA5 and AXA1 exhibit the lowest and highest PDP, respectively.

Figure 4 shows the number of transistors for each FA, as well the number of erronous



Figure 5: 8-to-4 Compressor Design

outputs. AXA2, InXA1 and InXA3 consist of 6 transistors each, and thus have a 78.6% area reduction compared to the exact MA. AMA5, AXA1, AXA3 and InXA2 all have 8 transistors. AMA5, AXA1 and AXA2 have 4 erroneous outputs. AMA3 and AMA4 have 3 erroneous outputs, and the remaining 6 designs have 2 erroneous outputs. Our results are consistent with the findings reported in [7] [8] [9].

Assuming that the characteristics of approximate FAs are linearly applied to approximate arithmetic circuits (adders and multipliers), there is no single approximate FA, which is superior in all aspects. Therefore, we propose to use a *fitness function* to evaluate the designs based on its design metrics.

$$Fitness = C1 * A + C2 * P + C3 * D + C4 * E + C5 * PDP$$
(1)

where C1, C2, C3, C4 and C5 are application-dependent design coefficients within the range [0,1] which provide weights to specific design metrics for a specific application, e.g., E equals zero for the exact designs where approximation is not allowed, and P is small for low power designs depending of application error-resiliency. The fitness of the approximate circuit depends on the application resiliency and input data distribution. A minimal fitness value is preferred since the goal is to minimize A, P, D and E. For the remainder of this work, we use all 11 Pareto-design approximate FAs as elementary building cells to construct approximate array multipliers.

Higher-order compressors, e.g., 5-to-3 (which compresses five partial product bits into three) and 8-to-4 (which compresses eight partial product bits into four) [13], allow us to construct high speed tree multipliers. Therefore, we also developed approximate FA based compressors, e.g., a 8-to-4 binary compressor is depicted in Figure 5, for evaluation purposes. Table 2 shows the power consumption and area for different approximate compressors implemented using approximate FAs. The area for approximate compressors exhibits a linear relationship with the area of FAs. However, it looks difficult to obtain a closed-form analytical expression for the power consumption. Few designs have a larger power consumption compared to the exact one, and this behavior needs more investigation. For that, and as a future work, we plan to use several ap-

 Table 2: Power Consumption and Area for Different Approximate Compressors based

 on Different Approximate FAs

i	Powe	r Consump	ption $(\mu w)$	ssors		Area (number of transistors)for Different Compressors							
		Compressor Type						ype					
FA Type	pe 3-2 4-3 5-3 6-3 7-3 8-4 FA Type						FA Type	3-2	4-3	5-3	6-3	7-3	8-4
Exact	0.562	1.469	1.659	1.466	1.355	2.198	Exact	28	56	70	98	112	154
M1	0.5474	0.9696	1.494	0.9258	1.138	1.65	M1	20	48	54	74	80	122
M2	0.4525	1.224	1.189	1.536	1.321	1.609	M2	14	42	42	56	56	98
M3	0.4489	0.6813	1.378	1.073	0.6157	0.9114	M3	11	39	36	47	44	86
M4	0.5228	0.9988	1.176	1.183	1.037	1.449	M4	15	43	44	59	60	102
M5	0.4802	0.9333	1.199	1.023	0.8753	1.791	M5	8	36	30	38	32	74
X1	0.4511	1.586	1.128	1.562	1.521	2.142	X1	8	36	30	38	32	74
X2	0.4584	1.296	1.563	0.8141	0.7489	2.77	X2	6	34	26	32	<b>24</b>	66
X3	0.3544	1.349	1.429	1.231	0.4742	2.316	X3	8	36	30	38	32	74
In1	0.1823	1.569	0.9423	0.4842	1.296	2.413	In1	6	34	26	32	<b>24</b>	66
In2	0.5018	1.324	2.114	0.3441	0.8087	3.844	In2	8	36	30	38	32	74
In3	0.5504	1.345	1.234	0.7866	1.636	5.27	In3	6	34	26	32	$\overline{24}$	66

proximate compressors with different approximation degrees in order to cover a larger design space. Considering all options, the total combination of compressor settings grows exponentially O( (# of FA designs)<sup># of FAs in compressor</sup>) = O  $(11)^4 = 14641$  in our case. Therefore, to show the effectiveness of designing approximate compressors based on approximate FAs, we chose four FAs only. These FAs have superior designs metrics. The best approximate FA in terms of delay and PDP was AMA5, and in terms of power and area was AXA2. Also, the best FA with low error rate was InXA1. AMA3 has moderate characteristics regarding area, power, delay, and number of errors. These selected FAs are used to design approximate high-order compressors, which in turn can be used for designing approximate tree multipliers. However, these selected compressors are not guaranteed to be the optimal ones. But, they exhibit some improvements compared to the exact designs.

### 4 Multiplier Basic Blocks

In this section, we use the approximate FAs and compressors, described above, to design 8x8 array and tree based multipliers, respectively. These 8x8 approximate multipliers will act as our basic blocks for designing higher-order multipliers, i.e., 32x32 and 64x64, as it will be discussed in Section 5.

### 4.1 8x8 Array Multiplier

An n-bit array multiplier [18] is composed of  $n^2$  AND gates for partial products generation, and n-1 n-bit adders for partial products accumulation. The design space of an  $n \ge n$  approximate array multiplier is quite huge, since it depends on the type of FA used in the array, and the *number* of approximate FAs (from 0 to n) used in the n-bit adder. Considering all options, the total combination of multiplier settings grow exponentially O( (# of FAs)<sup>MultiplierSize<sup>2</sup></sup>) = O ((11)<sup>n<sup>2</sup></sup>) = (11)<sup>64</sup> in our case.

Туре	MRED	MED	ER	NMED	Delay (ps)	$\begin{array}{c} \mathbf{Power} \\ (\mu \mathbf{W}) \end{array}$	size
EE	00	00	00	00	527	31.41	1456
EM1	8.55E-02	2.55E+02	9.70E-01	3.93E-03	527	24.17	1288
M1M1	2.13E+00	1.33E+04	9.96E-01	2.05E-01	865	14.75	1072
EM2	1.85E-01	2.29E+02	9.90E-01	3.52E-03	557	22.97	1162
M2M2	1.73E+01	1.68E + 04	1.00E+00	2.58E-01	600	14.4	784
EM3	4.03E-01	4.72E+02	9.99E-01	7.26E-03	605	24.95	1099
M3M3	1.25E+01	$1.72E{+}04$	1.00E+00	2.64E-01	598	15.31	640
EM4	3.64E-02	1.11E+02	9.70E-01	1.71E-03	573	21.85	1183
M4M4	6.11E-01	6.41E+03	9.96E-01	9.86E-02	313	11.17	832
EM5	3.03E-02	1.01E+02	9.30E-01	1.56E-03	573	22.15	1036
M5M5	6.76E-01	8.24E+03	9.90E-01	1.27E-01	250	10.69	496
EX1	1.18E-01	2.09E+02	9.71E-01	3.21E-03	546	31.86	1036
X1X1	2.84E+00	1.05E+04	9.96E-01	1.61E-01	558	21.33	496
EX2	1.09E-01	1.88E+02	1.00E+00	2.89E-03	569	23.38	994
X2X2	1.18E+01	$1.51E{+}04$	1.00E+00	2.31E-01	250	13.91	400
EX3	7.96E-02	3.48E+02	6.15E-01	5.35E-03	536	25.54	1036
X3X3	9.88E-01	1.63E+04	9.96E-01	2.50E-01	197	15.06	496
EIn1	7.50E-02	3.19E+02	6.15E-01	4.91E-03	517	26.07	994
In1In1	1.62E+00	1.02E+04	8.54E-01	1.56E-01	403	14.82	400
EIn2	3.68E-02	1.80E + 02	5.84E-01	2.76E-03	528	28.79	1036
In2In2	4.63E-01	8.28E+03	8.26E-01	1.27E-01	340	12.56	496
EIn3	1.85E-01	2.29E+02	9.90E-01	3.52E-03	556	27.96	994
In3In3	1.73E+01	1.68E + 04	1.00E+00	2.58E-01	404	23.92	400

Table 3: 8x8 Approximate Array Multiplier

We have used all 11 Pareto approximate FAs, described in Section 3, to construct 8x8 approximate array multipliers, based on only one FA type per design to avoid the exponential growth of the design space. Regarding the degree of approximation, we have used two options: i) all FAs are approximate, and ii) FAs that contribute to the least significant 50% of the resultant bits are approximated to maintain acceptable accuracy as recommended by [7] [12] [19]. Thus, we have designed, evaluated and compared 22 different options for building 8x8 approximate array multipliers as shown in Table 3, using the TSMC65nm technology. The type of the multiplier in Table 3 consists of two parts, i.e., the name of the adder used for the most significant and least significant part. For example, in EM1, the most significant part is based on an exact (E) adder and the least significant part is based on the mirror adder 1 (M1).

For our approximate designs, a specific approximation degree, from 1 to 2n, rather than n, may be chosen based on the maximum error allowed for a specific application, where in [20] [21], it is mentioned that it is suitable to chose a value of 10% for Maximum ED and 0.5% for MED. Figure 6 shows the ER, NMED and MRED for various 8x8 array multipliers. It is clear that fully approximate multipliers have high NMED. *EM5* has the lowest NMED, and *EM4* has a close-to-minimal NMED. Designs with high



NMED have a high MRED too. It can be observed that EIn2 exhibits the lowest ER. Also, EX3 and EIn1 have the same close-to-minimal ER.

Figure 6: ER  $x10^{-2}$ , NMED  $x10^{-3}$  and MRED  $x10^{-1}$  of 8x8 Array Multiplier



Figure 7: Area and PDP Reduction of 8x8 Array Multiplier

As shown in Table 3 and Figure 6, there is no single design that is superior in all design metrics. Therefore, a Pareto-analysis for the improvements in area and PDP is shown for the different designs proposed throughout this work. X3X3 has the lowest delay, and M5M5 and X2X2 also exhibit a low delay. M5M5, M4M4 and In2In2 exhibit the lowest power consumption among the 22 different designs. The size of the approximate multiplier exhibits a linear relationship with the degree of approximation. Thus, X2X2, In1In1 and In3In3, have the smallest size.

Figure 7 shows the area and PDP reduction of 8x8 array multipliers. The best designs are located on the bottom left corner. M5M5 is a Pareto-design with PDP reduction of 84% and area reduction of 65%. The design X3X3 is Non-Pareto because it has the same area reduction as the M5M5 but with a smaller PDP reduction. However, we have to consider other *error metrics*. Some designs such as EX1 have increased PDP due to excessive switching activity compared to the original design.

Type	MRED	MED	ER	NMED	Delay	Power	size
					(ps)	$(\mu \mathbf{W})$	
CEE	00	00	00	00	508	21.98	1218
CEM3	4.76E-01	6.05E+02	$1.00E{+}00$	9.30E-03	537	19.65	912
CM3M3	$1.06E{+}01$	1.41E+04	$1.00E{+}00$	2.16E-01	560	16.27	606
CEM5	4.76E-02	1.54E+02	9.79E-01	2.40E-03	356	18.63	858
CM5M5	5.16E-01	5.32E+03	9.99E-01	8.18E-02	282	13.99	498
CEX2	3.28E-01	3.68E+02	9.97E-01	5.70E-03	525	23.52	822
CX2X2	$7.35E{+}00$	8.95E+03	$1.00E{+}00$	1.38E-01	513	22.6	426
CEIn1	9.03E-02	3.10E+02	8.73E-01	4.80E-03	505	25.12	822
CIn1In1	5.08E-01	5.08E+03	9.75E-01	7.81E-02	500	26.89	426

 Table 4: 8x8 Approximate Tree Multiplier

#### 4.2 8x8 Tree Multiplier

The Wallace multiplier [22] is an efficient parallel multiplier that is composed of a tree of half adders (HAs) and FAs. The main idea is that, the adders in each layer operate in parallel without carry propagation until the generation of two rows of partial products. The design space for approximate 8x8 tree multipliers [22] is also quite large, depending on the *compressor type* and *approximation degree*. To avoid the exponentially growing design space, we choose to use compressors of the same type in the multiplier design. Also, we use two options for approximation degree: i) all compressors are approximate, and ii) compressors that contribute to the lowest significant 50% of the resultant bits are approximated to maintain an acceptable accuracy. Thus, based on the four shortlisted compressors, explained in Section 3, we compared 8 options for approximate 8x8 tree multipliers and the results are given in Table 4. The name of the multiplier consists of three parts. For example, CEM1 represents a compressor based multiplier (C), where the most significant part is based on an exact (E) compressor and the least significant part is composed of the mirror adder 1 (M1) based compressor. As shown in Table 4, there is no single design superior is all metrics, but some designs are the best wrt some few metrics.

Figure 8 shows the ER, NMED and MRED for various 8x8 tree multipliers. Fully approximate designs have higher NMED and MRED than partially approximate designs. The designs based on InX1 (*CEIn1* and *CIn1In1*) exhibit the lowest ER. *CM3M3* have the highest MRED. The designs based on *AMA5* have the lowest delay and power consumption due to their simple structures.

As depicted in Figure 9 which shows area and PDP reduction, the best designs are on the left bottom corner, i.e., *CM5M5* is a Pareto-design with maximum area and maximum PDP reduction. However, *CEM5* is a non Pareto-design because it has less reduction. Few designs on the right side of the figure have a PDP value greater than the exact design, which makes them unsuitable for low-power design usage.



Figure 8: ER  $x10^{-2}$ , NMED  $x10^{-3}$  and MRED  $x10^{-1}$  of 8x8 Tree Multiplier



Figure 9: Area and PDP Reduction of 8x8 Tree Multiplier

# 5 Higher-Order Multiplier Configuration

The 8x8 multiplier basic modules can be used to construct higher-order target multiplier modules. In this report, we use the example of designing a 16x16 multiplier to illustrate this process. The partial product tree of the 16x16 multiplication can be broken down into four products of 8x8 modules, which can be executed concurrently, as shown in Figure 10.



Figure 10: 16x16 Multiplier

In the case of high requirements of accuracy, an exact 8x8 multiplier can be used for the three most significant products, i.e., AHxBH, AHxBL, and ALxBH, and any one of the approximate designs can be used for the least significant product, i.e., ALxBL. For low accuracy requirements, only one 8x8 exact multiplier can be used for the most significant product, i.e., AHxBH, and any of the other approximate designs can be used for the three least significant products, i.e., AHxBL, ALxBH, and ALxBL. Modules that contribute to the lowest significant 50% of the resultant bits are approximated to maintain accuracy as recommended by [7] [12] [19] [23].

We choose to design 16x16 multipliers with an exact AHxBH multiplier, and with exact MSBs and approximate LSBs for AHxBL and ALxBH, and a fully approximate or approximate in LSBs only ALxBL. Any other approximation degree can be found based on the required quality function (maximum error, area, power or delay). Therefore, when the 16x16 multipliers are explained, the types of AHxBH, AHxBL and ALxBH are eliminated from the name, and only the type of ALxBL is used in the name of the multiplier.

#### 5.1 16x16 Array Multiplier

Table 5 shows the simulation results for 16x16 approximate array multipliers, which shows similarities with Table 3. The multiplier name is based on the type of ALxBL module. Figures 11, 12 and 13 show the ER, NMED and MRED for 16x16 array multipliers, respectively. It can be observed that 16M1M1 is the most accurate design with the lowest ER and lowest NMED. 16EIn2 is the second accurate design with low ER and NMED. For NMED, the best designs are 16M1M1, 16EIn2 and 16In2In2. Designs with high NMED show a high MRED value. EIn1In1 and 16In3In3 have the lowest delay. Fully approximate designs exhibit the minimal delay. Generally, designs based on approximate mirror adders have the lowest power consumption, due to the elimination of static power dissipation. Since, the design size grows linearly with the FA size, fully approximate designs based on 6 transistors cells including 16X2X2, 16In1In1 and 16In3In3 have the smallest number of transistors. Also, fully approximate designs including 16M5M5, 16X1X1, 16X3X3 and 16In2In2, based on 8 transistors FAs, have a very small size as well. Finally, the best designs regarding area reduction are 16In1In1, 16X2X2 and 16In3In3.



Figure 11: ER  $x10^{-2}$  of 16x16 Array Multiplier

As depicted in Figure 14 which shows the reduction in area and PDP for 16x16 array multipliers, the best designs are on the lower left corner, i.e., 16In1In1 and 16In3In3

Туре	MRED	MED	ER	NMED	Delay (ps)	$\begin{array}{c} \mathbf{Power} \\ (\mu \mathbf{W}) \end{array}$	size
16EE	00	00	00	00	514	156.8	5824
16EM1	1.19E-02	6.31E+04	9.44E-01	7.69E-10	534	130.1	5320
16M1M1	1.71E-04	1.33E+03	1.76E-02	1.10E-11	526	118.4	5104
16EM2	2.82E + 02	1.14E+05	1.00E+00	1.82E-05	533	128.4	4942
16M2M2	$3.53E{+}02$	1.33E+05	1.00E+00	2.28E-05	477	116.5	4562
16EM3	$9.53E{+}02$	3.34E+05	1.00E+00	6.16E-05	519	131.6	4753
16M3M3	$9.98E{+}02$	3.51E+05	1.00E+00	6.45E-05	490	120.4	4294
16EM4	7.80E-03	3.36E+04	9.29E-01	5.04E-10	522	118.8	5005
16M4M4	7.90E-03	3.32E+04	9.79E-01	5.11E-10	506	105.1	4654
$16 \mathrm{EM5}$	8.20E-03	4.06E+04	9.34E-01	5.30E-10	533	119	4564
16M5M5	8.20E-03	4.06E+04	9.34E-01	5.30E-10	535	105.1	4024
16EX1	1.15E-02	5.22E+04	9.51E-01	7.43E-10	513	154.9	4564
16X1X1	1.29E-02	5.74E+04	9.79E-01	8.34E-10	520	138.5	4024
16EX2	$9.40E{+}01$	5.96E + 04	1.00E+00	6.07E-06	521	138	4438
16X2X2	$1.41E{+}02$	6.85E+04	1.00E+00	9.11E-06	514	127.4	3844
16EX3	1.69E-02	9.09E+04	9.65E-01	1.09E-09	515	134	4564
16X3X3	1.97E-02	1.05E+05	9.79E-01	1.27E-09	518	121.8	4024
16EIn1	7.80E-03	4.57E+04	5.24E-01	5.04 E- 10	519	134.2	4438
16In1In1	8.40E-03	4.93E+04	6.09E-01	5.43E-10	408	121.7	3844
16EIn2	1.60E-03	8.08E+03	2.14E-01	1.03E-10	537	146.9	4564
16In2In2	2.20E-03	1.13E+04	4.29E-01	1.42E-10	500	126.4	4024
16EIn3	2.82E + 02	1.14E+05	1.00E+00	1.82E-05	527	157.6	4438
16In3In13	3.53E + 02	1.33E+05	1.00E+00	2.28E-05	412	153.2	3844

Table 5: 16x16 Approximate Array Multiplier



Figure 12: NMED x $10^{-5}$  of 16x16 Array Multiplier

are Pareto-designs while 16M4M4 is a non-Pareto design. Designs with negative PDP reduction values, indicate a power or delay larger than the exact design.



Figure 14: Area and PDP Reduction of 16x16 Array Multiplier

#### 5.2 16x16 Tree Multiplier

Table 6 depicts the characterization for 16x16 approximate tree multipliers, which to some degree shows similarities to Table 4. The design *16CM5M5* has the lowest power consumption. Figures 15, 16 and 17 shows the ER, NMED and MRED for 16x16 tree multipliers, respectively. *16CEIn1* and *16CIn1In1* have the lowest ER, delay and area. The same designs have high NMED and MRED. As depicted in Figure 18 which shows area and PDP reduction, the designs on the lower left corner are superior, i.e., *16CEM5*, *16CEIn1* and *16CM5M5* are all Pareto-designs while *16CEM3* is a non-Pareto design.

#### 5.3 Discussion and Comparison

The considered approximate multipliers are implemented using Cadence's Spectre based on TSMC65nm process, with  $V_{dd} = 1.0V$  at T=27C°. The circuit inputs are provided by independent voltage sources, and a load of 10fF is utilized. We evaluated and compared the design characteristics (Area, Power and Delay). As shown in Tables 3 and 4, the 8x8 exact tree multiplier exhibits lower delay, power and size compared to the exact 8x8 array multiplier.

Several multiplier designs, based on AMA5, have the lowest delay and power consumption, due to the basic structure of the FA cell, which is composed of two buffers

Туре	MRED	MED	ER	NMED	Delay (ps)	$\begin{array}{c c} \mathbf{Power} & \mathbf{size} \\ (\mu \mathbf{W}) & \end{array}$
16CEE	00	00	00	00	680	100.8 4872
16CEM3	1.07E+03	4.64E + 04	1.00E+00	3.00E-03	663	93.57 3954
16CM3M3	1.11E+03	4.80E+04	1.00E+00	3.10E-03	693	90.6 3648
16CEM5	9.10E-03	3.90E-01	9.41E-01	2.52E-08	585	92.48 3792
16CM5M5	9.30E-03	3.96E-01	9.79E-01	2.56E-08	670	86.98 3432
16CEX2	8.37E+02	$3.56E{+}04$	1.00E+00	2.30E-03	685	115   3684
16CX2X2	8.65E+02	3.71E + 04	1.00E+00	2.40E-03	671	114.3 3288
16CEIn1	1.74E-02	7.47E-01	8.22E-01	4.83E-08	516	112.5 3684
16CIn1In1	1.79E-02	7.70E-01	9.04E-01	4.98E-08	527	114.3   3288

Table 6: 16x16 Approximate Tree Multiplier



Figure 15: ER  $\rm x10^{-2}$  of 16x16 Tree Multiplier



Figure 16: NMED  $x10^{-3}$  of 16x16 Tree Multiplier

only. Also, they have the lowest NMED and a small size. Regarding accuracy, the designs based on *InXA1* have low ER and NMED. Similarly, the designs based on the 6 transistors FA, have the minimal size. Thus, it can be observed that the characteristics of approximate FA are generally propagated in the corresponding approximate multipliers as well.

In terms of architecture, we found that the tree multiplier designs tend to have a



Figure 18: Area and PDP Reduction of 16x16 Tree Multiplier

lower power consumption than array multipliers, especially the designs based on low power consumption FAs, such as AMA3 and AMA5. In terms of the 8x8 sub-module placement to form higher-order multipliers, with a fixed configuration for AHxBH, AHxBL and ALxBH sub-module, we have noticed that ER and NMED increase, while the size, power consumption and delay decrease for designs with a high degree of approximation in ALxBL.

Compared to the 24 different designs reported in [14], where 92% of the designs have ER close to 100%, only 80% of our proposed designs have high ER. Regarding NMED, almost all our designs have a value less than  $10^{-5}$ , which is the minimum value reported by the 24 approximate designs in [14]. Comparing the PDP reduction, most of the designs in [14] have a high PDP reduction because they are based on truncation and a high degree of approximation. However, our designs are superior in PDP reduction for designs with a high degree of approximation.

### 6 Application

While in previous sections, we used Cadence Spectre to build the circuits and evaluate their area, performance and power consumption. In this section, for experimentation purposes, we evaluate and compare the accuracy of the built approximate multipliers



Figure 19: Image blinding

based on an image blending application, where two images are multiplied pixel-bypixel as shown in Figure 19. Here, we use MATLAB to evaluate error metrics for image processing. To this end, we have modeled the same approximate multiplier circuit architectures in MATLAB and run exhaustive simulation.

The signal to noise ratio (SNR) is used to measure the image quality. Figure 20 shows a comparison of the SNR and the percentage of PDP reduction for different approximate multipliers. Designs on the bottom left corner, have the highest PDP reduction and the best quality (high SNR). Generally, all multiplier designs have an acceptable SNR (acceptable quality). However, there exist some designs, e.g., 16EIn3, 16CEX2 and 16CX2X2, with PDP greater than the exact design. The library of implemented cells and multiplier circuits, and the results of the image blending application can be found at https://sourceforge.net/projects/approximatemultiplier.



Figure 20: %PDP Reduction and SNR of Multipliers

# 7 Conclusions

In this report, we designed, evaluated and compared different approximate multipliers, based on approximation in partial product summation. The design space of approx-

imate multipliers is found to be primarily dependent on the type of the approximate FA used, the architecture, and the placement of 8x8 sub-modules in the higher-order nxn multipliers. The proposed designs are compared based on PDP, area, delay, power, quality (ER, NMED and MRED). Various optimal designs have been identified in terms of the considered design metrics. An image blending application is used to compare the proposed multiplier designs in terms of SNR and PDP. Our designs show comparative results compared to 24 different approximate designs reported in [14]. In the future, we plan to investigate the design space of higher-order multiplier modules (e.g., 64x64) using the already considered metrics and configurations. Moreover, we also plan to evaluate the possibility of having mixed FAs in the 8x8 multiplier block.

### References

- J. Han and M. Orshansky, "Approximate computing: An emerging paradigm for energy-efficient design," in *European Test Symposium*, 2013, pp. 1–6.
- [2] P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an underdesigned multiplier architecture," in *VLSI Design*, 2011, pp. 346–351.
- [3] A. K. Verma, P. Brisk, and P. Ienne, "Variable latency speculative addition: A new paradigm for arithmetic circuit design," in *Design*, *Automation Test in Europe*, 2008, pp. 1250–1255.
- [4] N. Zhu, W. L. Goh, and K. S. Yeo, "An enhanced low-power high-sspeed adder for error-tolerant application," in *Integrated Circuits*, 2009, pp. 69–72.
- [5] K. Du, P. Varman, and K. Mohanram, "High performance reliable variable latency carry select addition," in *Design, Automation Test in Europe*, 2012, pp. 1257–1262.
- [6] H. Jiang, J. Han, and F. Lombardi, "A comparative review and evaluation of approximate adders," in *Great Lakes Symposium on VLSI*. ACM, 2015, pp. 343–348.
- [7] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 1, pp. 124–137, 2013.
- [8] Z. Yang, A. Jain, J. Liang, J. Han, and F. Lombardi, "Approximate xor/xnorbased adders for inexact computing," in *Nanotechnology*, 2013, pp. 690–693.
- [9] H. A. F. Almurib, T. N. Kumar, and F. Lombardi, "Inexact designs for approximate low power addition by cell replacement," in *Design*, Automation Test in Europe, 2016, pp. 660–665.
- [10] K. Y. Kyaw, W. L. Goh, and K. S. Yeo, "Low-power high-speed multiplier for error-tolerant application," in *Electron Devices and Solid-State Circuits*, 2010, pp. 1–4.
- [11] G. Zervakis, K. Tsoumanis, S. Xydis, D. Soudris, and K. Pekmestzi, "Designefficient approximate multiplication circuits through partial product perforation," vol. 24, no. 10, 2016, pp. 3105–3117.
- [12] K. M. Reddy, Y. B. N. Kumar, D. Sharma, and M. H. Vasantha, "Low power, high speed error tolerant multiplier using approximate adders," in VLSI Design and Test, 2015, pp. 1–6.
- [13] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and analysis of approximate compressors for multiplication," in *IEEE Transactions on Computers*, vol. 64, no. 4, 2015, pp. 984–994.

- [14] H. Jiang, C. Liu, N. Maheshwari, F. Lombardi, and J. Han, "A comparative evaluation of approximate multipliers," in *Nanoscale Architectures*, 2016, pp. 191– 196.
- [15] R. Hrbacek, V. Mrazek, and Z. Vasicek, "Automatic design of approximate circuits by means of multi-objective evolutionary algorithms," in *Design and Technology* of Integrated Systems, 2016, pp. 1–6.
- [16] Z. Yang, J. Yang, K. Xing, and G. Yang, "Approximate compressor based multiplier design methodology for error-resilient digital signal processing," in 2016 IEEE International Conference on Signal and Image Processing (ICSIP), 2016, pp. 740–744.
- [17] S. Rehman, W. El-Harouni, M. Shafique, A. Kumar, and J. Henkel, "Architectural-space exploration of approximate multipliers," in *CAD*. ACM, 2016, pp. 1–8.
- [18] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*. Prentice-Hall, 2002.
- [19] B. Shao and P. Li, "Array-based approximate arithmetic computing: A general model and applications to multiplier and squarer design," vol. 62, no. 4, 2015, pp. 1081–1090.
- [20] S. Venkataramani, A. Sabne, V. Kozhikkottu, K. Roy, and A. Raghunathan, "SALSA: Systematic logic synthesis of approximate circuits," in *Design Automation Conference*, 2012, pp. 796–801.
- [21] S. Venkataramani, K. Roy, and A. Raghunathan, "Substitute-and-simplify: A unified design paradigm for approximate and quality configurable circuits," in *Design, Automation Test in Europe*, 2013, pp. 1367–1372.
- [22] B. Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*. Oxford University Press, 2010.
- [23] D. Sengupta and S. S. Sapatnekar, "FEMTO: Fast error analysis in multipliers through topological traversal," in *International Conference on Computer-Aided Design*, 2015, pp. 294–299.